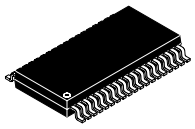


SLUS522A – JANUARY 2002 – REVISED SEPTEMBER 2002

Cool-GG™ PROGRAMMABLE BATTERY MANAGEMENT IC

FEATURES

- **Powerful Low-Power 8-Bit RISC CPU Core Operating at up to 4 MHz Clock Frequency**
- **Flexible Memory Architecture**
  - **16k × 22 Program Flash EPROM**
  - **4k × 22 Program Mask ROM**
  - **512 × 8 Data Flash EPROM**
  - **512 × 8 Data RAM**
- **Three Reduced Power Modes**
  - **Low Power: <240 μA**
  - **Sleep: < 8 μA**
  - **Hibernate: <0.5 μA**
- **High-Accuracy Analog Front End With Two Independent ADCs**
  - **High-Resolution Integrator for Coulomb Counting—Better Than 3nVh Resolution**
  - **Coulomb Counter Self-Calibration Reduces Offset to Less Than 1 μV**
  - **15-Bit Delta-Sigma ADC With a 12-Channel Multiplexer for Voltage, Current, and Temperature Measurements**
- **Accurate On-Chip 32.768-kHz Oscillator**
- **Internal Clock Synthesizer Generates Frequencies up to 4 MHz**
- **Integrated Flash Memory Eliminates Need for External EEPROM**
- **24 Memory-Mapped I/O Pins**
- **Supports Two Serial Communication Protocols**
  - **Two-Wire SMBus v1.1 Interface**
  - **Single-Wire HDQ Interface**
- **Package: 38-Pin TSSOP (DBT)**
- **Complete Integrated Development Environment**

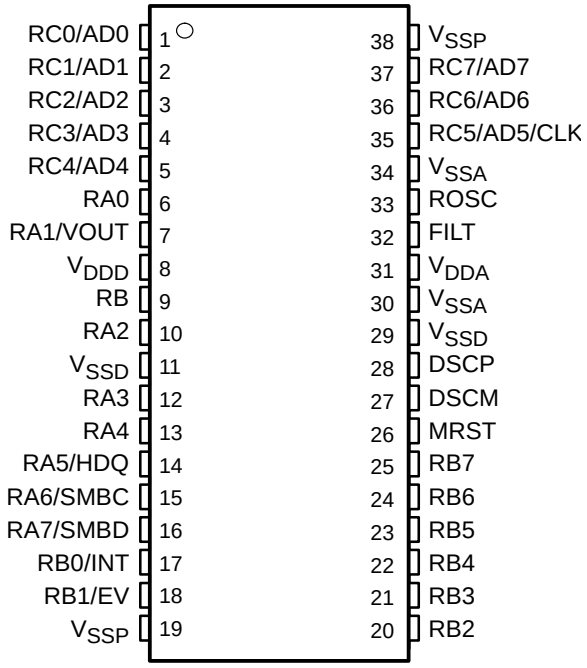
APPLICATIONS

- **Battery Management**
- **Gas Gauges**

DESCRIPTION

The Texas Instruments bq8015 *Cool-GG*™ programmable battery management IC is the next in a series of advanced, high-performance, reduced-instruction-set-CPU (RISC) integrated circuits for battery management and gas-gauge applications. In a single CMOS IC, the bq8015 combines high-accuracy analog measurement capabilities with a low-power high-speed RISC processor, integrated flash memory, and an array of peripheral and communication ports. The program flash EPROM allows fast development of custom implementations, and the low-power analog peripherals improve accuracy beyond discrete implementations. In its 38-pin TSSOP package, the bq8015 can implement a variety of functions in a small PCB area.

TSSOP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DSCM	27	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between DSCP and DSCM. DSCM can also be selected as an input to the over-sampled ADC.
DSCP	28	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between DSCP and DSCM. DSCP can also be selected as an input to the over-sampled ADC.
FILT	32	IA	Analog pin connected to the external PLL loop filter components
MRST	26	I	Master reset input pin that forces the device into reset when held high. Must be held low for normal operation.
RA0	6	I/OD	Port A.0 digital open-drain I/O pin
RA1/VOUT	7	I/O	Port A.1 digital push-pull I/O pin with pullup capable of driving power for an external device
RA2	10	I/OD	Port A.2 digital open-drain I/O pin
RA3	12	I/OD	Port A.3 digital open-drain I/O pin
RA4	13	I/OD	Port A.4 digital open-drain I/O pin
RA5/HDQ	14	I/OD	Port A.5 digital open-drain I/O pin or one-wire DQ/HDQ serial communication pin
RA6/SMBC	15	I/OD	Port A.6 digital open-drain I/O pin or SMBus clock pin
RA7/SMBD	16	I/OD	Port A.7 digital open-drain I/O pin or SMBus data pin
RB	9	P	RAM backup pin to provide backup potential to the internal DATA RAM if V_{CC} is momentarily shorted, by using a capacitor attached between RB and V_{SS}
RB0/INT	17	I/OD	Port B.0 digital open-drain I/O pin or selectable as a configurable external processor interrupt
RB1/EV	18	I/OD	Port B.1 digital open-drain I/O pin or selectable as a configurable external event input to wake the controller from a halt state
RB2	20	I/OD	Port B.2 digital open-drain I/O pin
RB3	21	I/OD	Port B.3 digital open-drain I/O pin
RB4	22	I/OD	Port B.4 digital open-drain I/O pin
RB5	23	I/OD	Port B.5 digital open-drain I/O pin
RB6	24	I/OD	Port B.6 digital open-drain I/O pin
RB7	25	I/OD	Port B.7 digital open-drain I/O pin
RC0/AD0	1	I/O	Port C.0 digital push-pull I/O pin or selectable as an input, AD0, to the over-sampled ADC
RC1/AD1	2	I/O	Port C.1 digital push-pull I/O pin or selectable as an input, AD1, to the over-sampled ADC
RC2/AD2	3	I/O	Port C.2 digital push-pull I/O pin or selectable as an input, AD2, to the over-sampled ADC
RC3/AD3	4	I/O	Port C.3 digital push-pull I/O pin or selectable as an input, AD3, to the over-sampled ADC
RC4/AD4	5	I/O	Port C.4 digital push-pull I/O pin or selectable as an input, AD4, to the over-sampled ADC
RC5/AD5/CLK	35	I/O	Port C.5 digital push-pull I/O pin or selectable as an input, AD5, to the over-sampled ADC or a 32-kHz square-wave output
RC6/AD6	36	I/O	Port C.6 digital push-pull I/O pin or selectable as an input, AD6, to the over-sampled ADC
RC7/AD7	37	I/O	Port C.7 digital push-pull I/O pin or selectable as an input, AD7, to the over-sampled ADC
ROSC	33	IA	Internal oscillator bias resistor input pin
V_{DDA}	31	P	Positive supply for analog circuitry. V_{DDA} and V_{DDD} must be driven to the same potential.
V_{DDD}	8	P	Positive supply for digital circuitry and I/O pins. V_{DDD} and V_{DDA} must be driven to the same potential.
V_{SSA}	30, 34	P	Negative supply for analog circuitry. V_{SSA}, V_{SSD}, and V_{SSP} must be driven to the same potential.
V_{SSD}	11, 29	P	Negative supply for digital circuitry. V_{SSA}, V_{SSD}, and V_{SSP} must be driven to the same potential.
V_{SSP}	19, 38	P	Negative supply for output circuitry. V_{SSA}, V_{SSD}, and V_{SSP} must be driven to the same potential.

NOTE: I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = power

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} relative to V_{SS} (see Note 1) . . . . . –0.3 V to 6 V
Open-drain I/O pins, $V_{(IOD)}$ relative to V_{SS} (see Note 1) . . . . . –0.3 V to 6 V
Input voltage range to all other pins, V_I relative to V_{SS} (see Note 1) . . . . . –0.3 V to V_{DD} + 0.3V
Operating free-air temperature range, T_A . . . . . –20°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
ESD Rating (see Note 2) HBM . . . . . 1.5 kV
CDM . . . . . 1.5 kV
MM . . . . . 50 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. V_{SS} refers to the common node of $V_{(SSA)}$, $V_{(SSD)}$, and V_{SS}.
2. Design considerations should be made with respect to excessive ESD.

electrical characteristics, T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DDD)}$	Digital supply voltage range		3	3.3	3.6	V
$V_{(DDA)}$	Analog supply voltage range		3	3.3	3.6	
$I_{(DDD)}$	Digital supply current	Normal (see Note 3)		1.7	2	mA
		Low power (see Note 4)		13	30	µA
		Sleep (see Note 5)		0.3	1	
		Hibernate (see Notes 6, 7)		0.05	0.2	
$I_{(DDA)}$	Analog supply current	Normal (see Note 3)		315	400	
		Low power (see Note 4)		240	310	
		Sleep (see Note 5)		8	13.5	
		Hibernate (see Notes 6, 7)		0.4	0.8	
$I_{(DDPOR)}$	Power on reset current	$V_{(DD)} < V_{(POR)}$		0.01	0.5	

NOTES: 3. CPU executing. No flash programming or erase operation .ADC and CC operating. VOUTEN = 0.
4. Oscillator, PLL and POR circuits active (PLL_OFF=0, LP_CLK=1, OSC_EN=1) CC operating. CPU halted.
5. Oscillator and POR circuits active, PLL is off (PLL_OFF=1, LP_CLK=1, OSC_EN=1) CPU halted.
6. POR circuit active. Oscillator and PLL are off. (PLL_OFF=1, LP_CLK=1, OSC_EN=0). CPU halted.
7. $I_{(DDD)} + I_{(DDA)} \leq 1$ µA

electrical characteristics, T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted) (continued)

power-on reset (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT-}	Negative-going voltage input		2.1	2.3	2.5	V
V_{hys}	Hysteresis voltage		50	125	200	mV

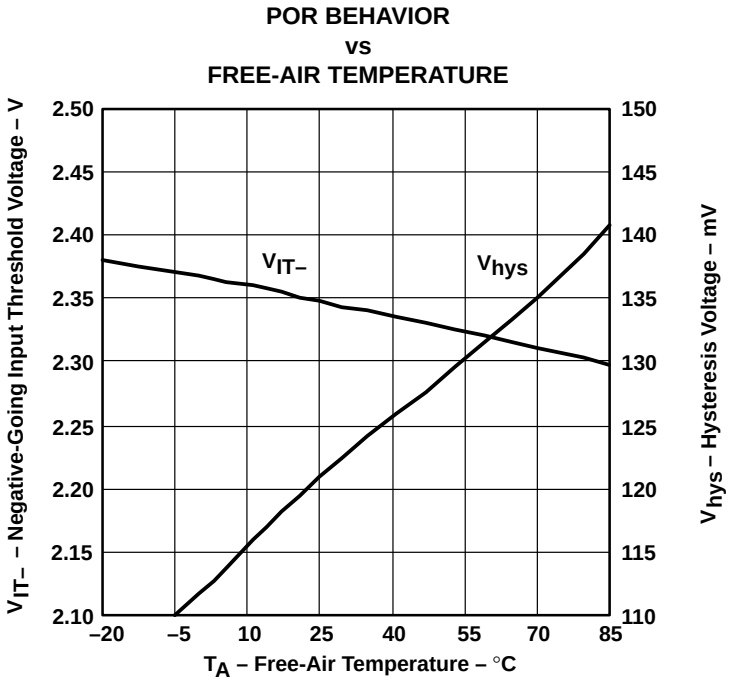


Figure 1

general purpose digital inputs and outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage low				0.8	V
V_{OH}	Output voltage† high	I_L =–0.5 mA	V_{DD}–0.5			V
V_{OL}	Low-level output voltage	I_L = 0.5 mA			0.4	V
C_I	Input capacitance			5		pF
I_{OL}	Low-level output current	Open drain outputs, V_{OL} = 0.4 V			10	mA
$I_{(VOUT)}$	VOUT source current	VOUT active, V_{OUT} = V_{DD} –0.6 V	–5			mA
$I_{lkg(VOUT)}$	VOUT leakage current	VOUT inactive	-0.2		0.2	µA
I_{lkg}	Input leakage current				1	µA

† RC[0:7] bus

electrical characteristics, T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted) (continued)

ADC (Unless otherwise specified, the specification limits are valid at both slow and fast modes as well as internal and external reference.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	Internal V_{ref}	–0.3		1	V
	External V_{ref}	–0.3		0.8×V_{DDA}	
Conversion time	FAST = 0		31.5		ms
	FAST = 1		2.0		
Resolution (no missing codes)	FAST = 0	16			bits
Effective resolution	FAST = 0	14	15		bits
	FAST = 1	9	10		
Input referred noise	FAST = 0		20		μV_{rms}
	FAST = 1		375		
Integral nonlinearity	FAST = 0, –0.1 V to 0.8 x V_{ref}		±0.003	±0.009	%FSR†
	FAST = 0, –0.3 V to –0.1 V		±0.043		
	FAST = 1, –0.1 V to 0.8 x V_{ref}		±0.008	±0.016	
	FAST = 1, –0.3 V to –0.1 V		±0.043		
Offset error	FAST = 0		100	250	µV
Offset error drift	FAST = 0; typical 25–70°C		475	4000	nV/°C
Full-scale error‡			±0.25%		
Full-scale error drift	FAST = 0		150		PPM/°C
Effective input resistance§		8			MΩ

† Full-scale reference
‡ Uncalibrated performance. This gain error can be eliminated with external calibration.
§ The A/D input is a switched-capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.

coulomb counter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		-0.3		1.0	V
Conversion time	Single conversion		250		ms
Effective resolution (see Note 8)	Single conversion	15			bits
Noise	Single conversion		20		µVrms
Integral nonlinearity	–0.1 V to 0.8 x V_{ref}		±0.003	±0.009	%FSR
	–0.3 V to –0.1 V		±0.043		
Offset error (see Note 8)			1		µV
Offset error drift			0.4	3	µV/°C
Full-scale error			±0.25%		
Full-scale error drift	25°C–70°C typical		150		PPM/°C
Effective input resistance		10			MΩ

NOTE 8: Post-calibration performance

electrical characteristics, T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted) (continued)

temperature sensor (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$ Temperature sensor voltage (see Note 9)			–2.2		mV/°C

NOTE 9: –58.6 LSB/°C

TEMPERATURE SENSOR VOLTAGE
vs
FREE-AIR TEMPERATURE

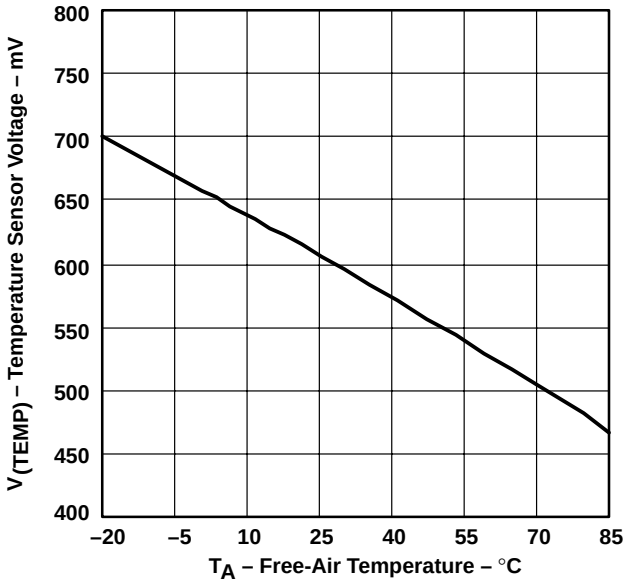


Figure 2

electrical characteristics, T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted) (continued)

voltage reference (see Figure 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage		1.2128	1.225	1.2373	V
Output voltage drift	Over 50°C		40		PPM/°C

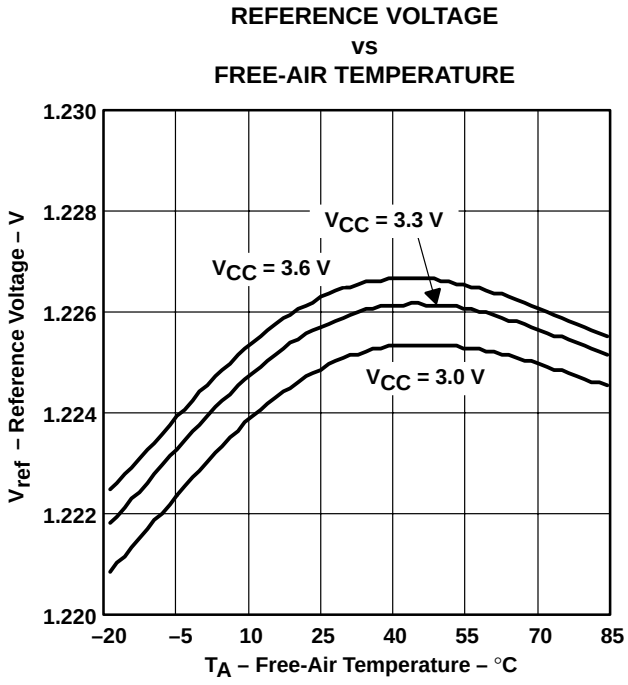


Figure 3

PLL switching characteristics, T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(sp)}$ Start-up time (see Note 10)	±0.5% frequency error		2.0	5.0	ms

NOTE 10: The frequency error is measured from 32768 Hz.

electrical characteristics, T_A = –20°C to 85°C, 3 V to 3.6 V (unless otherwise noted) (continued)

internal oscillator (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(exo)}$	Frequency error (see Note 11)		–2%	0.5%	2%	
$t_{(sxo)}$	Start-up time (see Note 12)				250	μs

NOTES: 11. The frequency error is measured from 32768 Hz.
12. The startup time is defined as the time it takes for the oscillator output frequency to be ±2%.

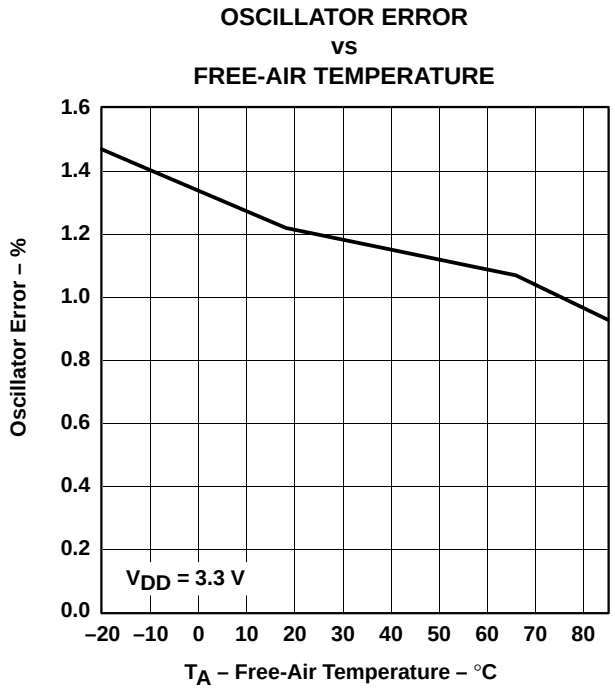


Figure 4

data flash memory switching characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention	See Note 13	10			Years
	Flash programming write-cycles	See Note 13		10^5		Cycles
$t_{(ROWPROG)}$	Row programming time	See Note 13			2	ms
$t_{(MASSERASE)}$	Mass-erase time	See Note 13			4	ms
$I_{(DDPROG)}$	Flash-write supply current	See Note 13		14	16	mA
$I_{(DDERASE)}$	Flash-erase supply current	See Note 13		14	16	mA

NOTE 13: Assured by design. Not production tested.

register backup

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RB)}$	RB data-retention input current (see Note 14)	$V_{RB} > 3.0$ V, $V_{DD} < V_{IT}$		10	100	nA
$V_{(RB)}$	RB data-retention voltage		1.3			V

NOTE 14: Assured by design. Not production tested.

SMBus timing characteristics, $T_A = -20°C$ to $85°C$, $3.0\ V < V_{CC} < 3.6\ V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
F_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
T_{BUF}	Bus free time between start and stop (see Figure 5)		4.7			µs
$T_{HD:STA}$	Hold time after (repeated) start (see Figure 5)		4.0			µs
$T_{SU:STA}$	Repeated start setup time (see Figure 5)		4.7			µs
$T_{SU:STO}$	Stop setup time (see Figure 5)		4.0			µs
$T_{HD:DAT}$	Data hold time (see Figure 5)	Receive mode	0			µs
		Transmit mode	300			
$T_{SU:DAT}$	Data setup time (see Figure 5)		250			µs
$T_{TIMEOUT}$	Error signal/detect (see Figure 5)	See Note 15	25		35	ms
T_{LOW}	Clock low period (see Figure 5)		4.7			µs
T_{HIGH}	Clock high period (see Figure 5)	See Note 16	4.0		50	µs
$T_{LOW:SEXT}$	Cumulative clock low slave extend time	See Note 17			25	ms
$T_{LOW:MEXT}$	Cumulative clock low master extend time (see Figure 5)	See Note 18			10	ms
T_F	Clock/data fall time	See Note 19			300	ns
T_R	Clock/data rise time	See Note 20			1000	ns

NOTES: 15. The bq8015 times out when any clock low exceeds $T_{TIMEOUT}$

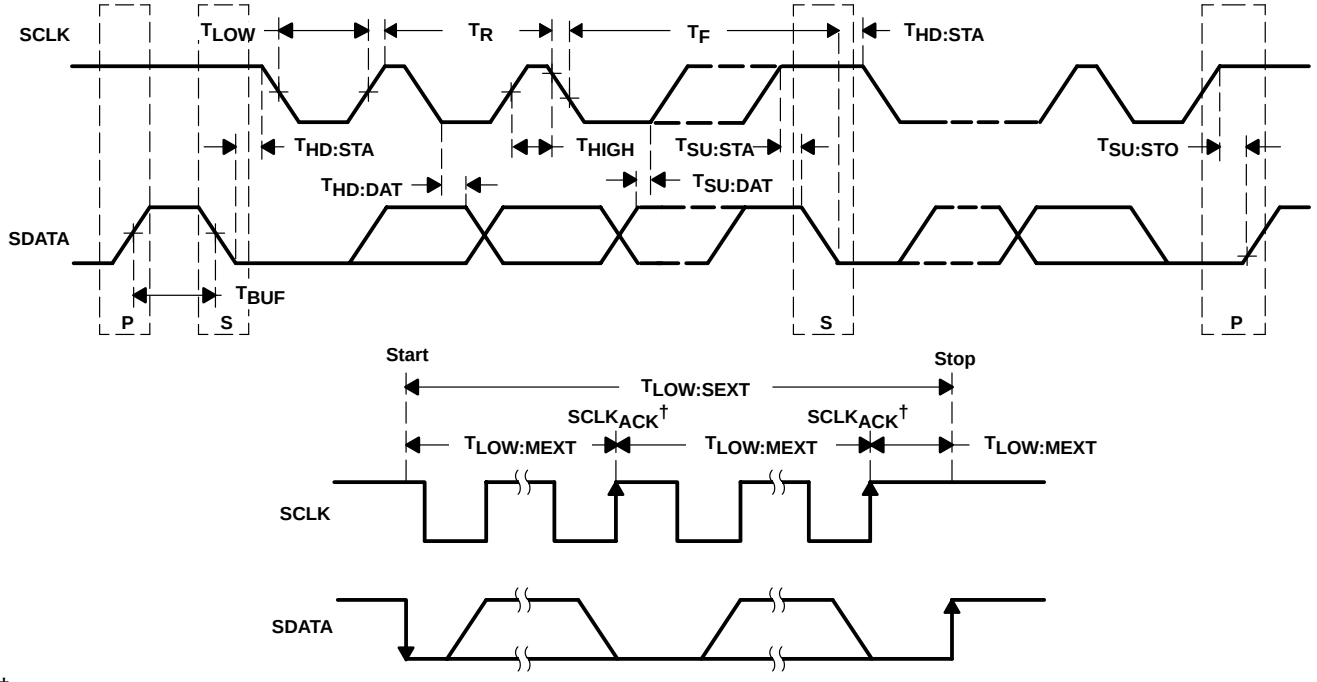
16. $T_{HIGH, Max}$, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 µs causes reset of any transaction involving bq8015 that is in progress.
17. $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
18. $T_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
19. Rise time $T_R = V_{ILMAX} - 0.15)$ to $(V_{IHMIN} + 0.15)$
20. Fall time $T_F = 0.9V_{DD}$ to $(V_{ILMAX} - 0.15)$

HDQ timing characteristics, T_A = –20°C to 85°C, 3.0 V < V_{CC} < 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(CYCH)}$	Cycle time, host to bq8015 (write)	See Figure 7	190			µs
$t_{c(CYCB)}$	Cycle time, bq8015 to host (read)	See Figure 8	190	205	250	µs
$t_{h(STRH)}$	Start hold time, host to bq8015 (write)	See Figure 7	5			ns
$t_{h(STRB)}$	Start hold time, host to bq8015 (read)	See Figure 8	32			µs
$t_{su(DSU)}$	Data setup time	See Figure 7			50	µs
$t_{su(DSUB)}$	Data setup time	See Figure 8			50	µs
$t_{h(DH)}$	Data hold time	See Figure 7	100			µs
$t_{(DV)}$	Data valid time	See Figure 8	80			µs
$t_{su(SSU)}$	Stop setup time	See Figure 7			145	µs
$t_{su(SSUB)}$	Stop setup time	See Figure 8			145	µs
$t_{(RSPS)}$	Response time, bq8015 to host		190		320	µs
$t_{(B)}$	Break time	See Figure 6	190			µs
$t_{(BR)}$	Break recovery time	See Figure 6	40			µs

Figures 5–8 are timing diagrams for the bq8015.

SMBus timing diagrams



† $SCLK_{ACK}$ is the acknowledge-related clock pulse generated by the master.

Figure 5. SMBus Timing Diagram

HDQ timing diagrams

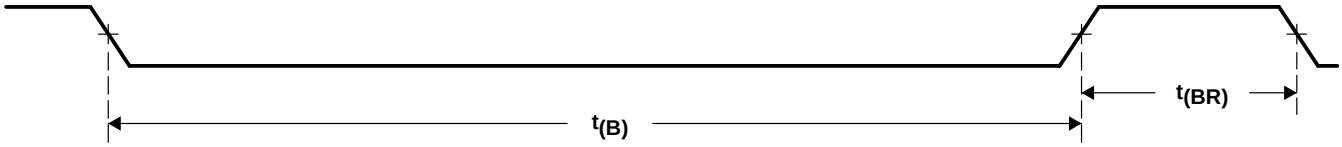


Figure 6. HDQ Break Timing

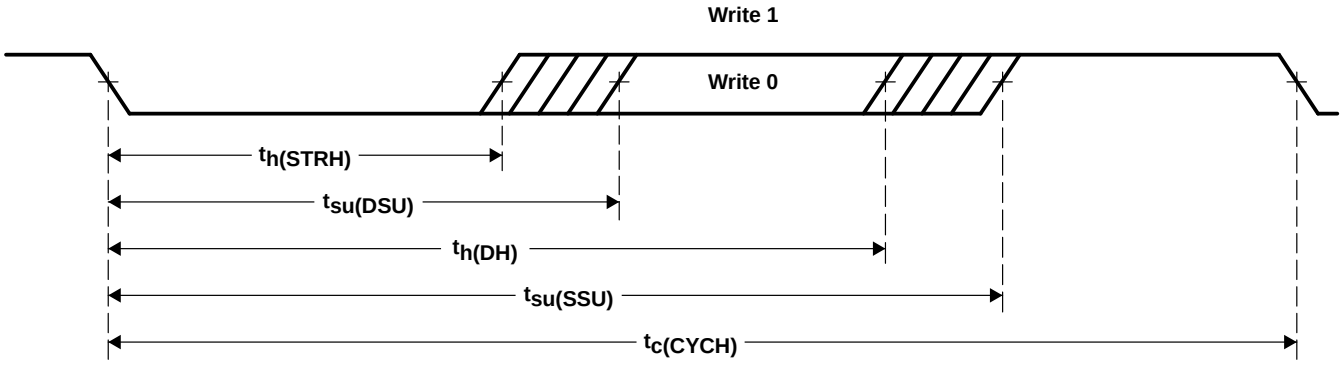


Figure 7. HDQ Host to bq8015

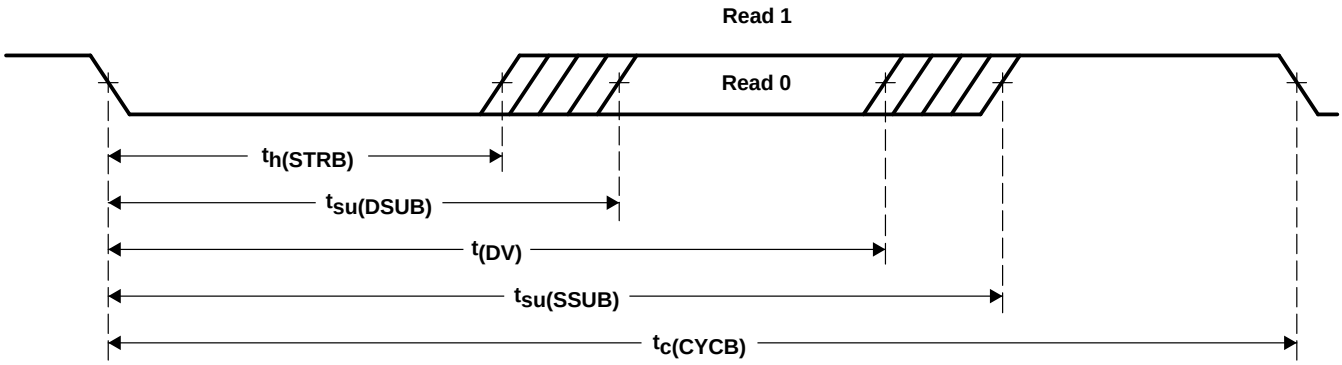
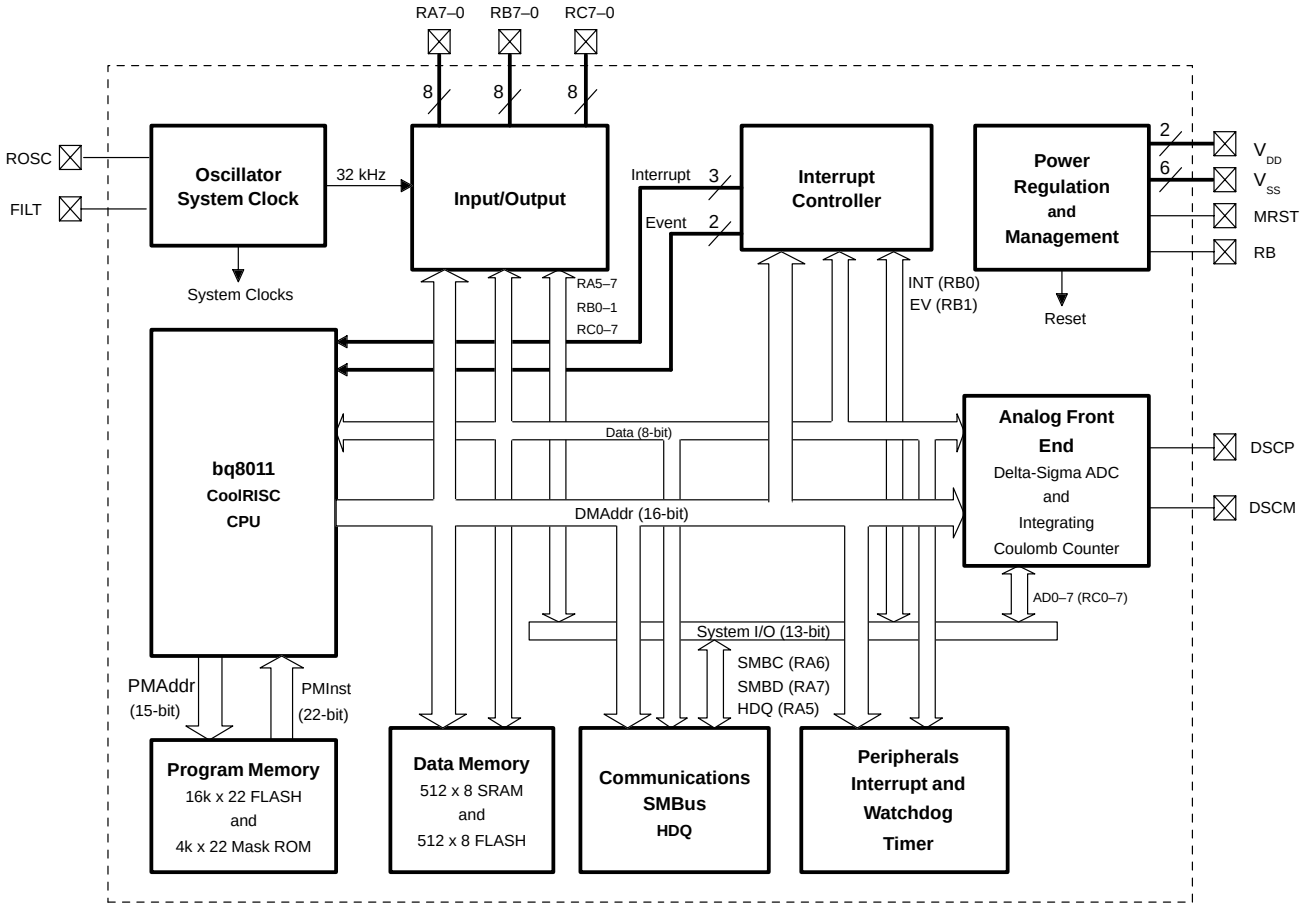


Figure 8. HDQ bq8015 to Host

functional block diagram



general operational overview

The bq8015 functional block diagram outlines the major components within the IC. Together with the flash-based firmware, the bq8015 performs the necessary calculations and control for a fully functional battery management system. Each of the major component blocks in the bq8015 is outlined below.

RISC processor

The bq8015's flexible architecture allows easy development of numerous battery-management solutions. Based on a RISC processor featuring a Harvard architecture, the bq8015 operates at frequencies up to 4 MHz. The clock frequency is synthesized from an internal 32 kHz oscillator and is programmable under firmware control. Using a three-stage instruction pipeline, the RISC processor can execute one instruction every clock cycle. With a 22-bit instruction width, the bq8015 can manipulate complex data with a single line of code. Further details about the bq8015 core architecture and CPU instruction set are in the bq80xx Core Manual.

general operational overview (continued)

data and program memory

To improve performance and reduce operating power, the bq8015 uses separate data and program memory address busses, providing ample program and data-storage capability. This feature also allows for future memory expansion of the bq8015 family without affecting existing programs.

The bq8015 provides 512 bytes of data RAM on two 256-byte pages and another 512 bytes of flash EPROM on another two 256-byte pages. The flash EPROM is available to store user specific static data, such as serial numbers and system operational data, without modifying the program memory. The bq8015 provides flexible instruction memory for implementing a wide-variety of battery management functions. For better flash EPROM utilization, the bq8015 instruction memory is separated into two blocks. The first block is a 16k x 22 flash EPROM for custom user programs and the second block is a 4k x 22 mask ROM containing common programs such as the math and battery-management libraries, communication, and power-on reset routines. Refer to the bq8015 Mask ROM description for further details.

In addition, the 512 bytes of general-purpose SRAM can be powered by the RB pin of the bq8015 if power is lost. Typically, a capacitor provides the necessary voltage to the cells during inadvertent power loss. The RB pin can also be connected to a battery cell to provide power to the DATA RAM for longer periods. The RB pin operating current is less than 50 nA.

Figures 6 and 7 outline the bq8015 memory maps and show the address location of the internal registers. Further details about the bq8015 registers are in the register description section and Table 1, bq8015 Register and Peripheral Map.

analog front end

The bq8015 features a precision analog front end ideal for battery monitoring and capacity measurement applications. Two analog-to-digital converters (ADCs) and a 12-channel multiplexer are available, allowing program flexibility. The first ADC is an integrating converter designed specifically for coulomb counting. The converter resolution is a function of how many samples are integrated: 16 samples for 10 μV resolution. For example, 37.4 μV can be resolved in 250 ms. Therefore, a 10 μV signal is resolved in approximately 4 seconds. The second converter is a 15-bit delta sigma ADC for general-purpose measurements. This converter can be connected to one of eight multiple-purpose I/O pins, an internal temperature sensor, the current sense inputs, or the negative power supply. The 15-bit mode has a conversion time of 32 ms and the 10-bit mode has a conversion time of 2 ms. In either mode, a full 16 bits are returned from the converter for better averaging capability.

I/O and specialized functions

The bq8015 provides a total of 24 memory-mapped I/O lines in three ports (A, B, C). These ports are used for data conversion, communication, external device power interface, external interrupt or wake, and general-purpose control functions.

The bq8015 provides two hardware communications ports. The first is the two-wire SMBus interface (SMBC and SMBD, dual function with RA6 and RA7). Together with the proper firmware, this communication port is compatible with the SMBus v1.1 protocol supporting packet error check (PEC) if enabled. The second communication is the single-wire HDQ serial interface (dual function with RA5). This pin can be made to support HDQ8 (8-bit) or HDQ16 (16-bit) protocols found on other bq gas gauge and battery management devices.

VOUT (Dual function with RA1) is a switch power supply of up to 5mA to an external device under bq8015 firmware control. This power supply reduces the system implementation requirements for powering devices external to the bq8015 and eliminates wasting the additional power when the external device is not needed.

I/O and specialized functions (continued)

Clock out (32-kHz output) is dual-functioned with RC5. The 32-kHz output can be used to provide an accurate time base to external devices such as a lithium-ion protector IC without the cost of generating a new clock. The 32 kHz clock within the bq8015 simplifies the implementation.

The interrupt pin (dual function with RB0) provides a hardware means of interrupting the bq8015 during operation. The event pin (dual function with RB1) provides a hardware means of waking the bq8015 during sleep or hibernate modes. The inputs, if enabled, signal the CPU to resume from a HALT state.

Further information about the specialized port functions is given in the bq8015 device pin-out and pin descriptions. Using the special functions is detailed in the register map and register details section.

An internal temperature sensor is available on the bq8015 to reduce the cost, power, and size of the external components necessary to measure temperature. Scaled to –58.6 LSB/°C in the ADHI and ADLO registers, the internal temperature sensor is ideal for determining pack temperature during storage and the IC temperature during operations.

power consumption

The bq8015 core running from the mask ROM is capable of 1,700 MIPS/Watt in a 3 V system. Combined with other very low power analog peripherals, the bq8015 is ideal for embedded battery management applications. The bq8015 also provides three reduced-power modes for additional power savings. In the low-power mode, the CPU is halted but the PLL and clock oscillator are still operating. In the sleep mode, the CPU is halted, the PLL is off, and the clock oscillator is running. In this mode, the current is less than 8 μA. In the hibernate-mode, the CPU is halted, and both the PLL and clock oscillator are turned off, reducing the current to less than 1 μA.

mask ROM functions

The bq8015 default-state is with the flash EPROM programmed to all 1s. Upon powering up the bq8015 for the first time, the initialization routine is executed from the mask ROM. After initialization, the bq8015 defaults as an SMBus slave (address 16h). From this point, the flash instruction memory may be programmed. Once the flash programming is complete and the proper commands initiated, the bq8015 executes its program from the flash memory. During normal operation, the library commands in the mask ROM are still available for use.

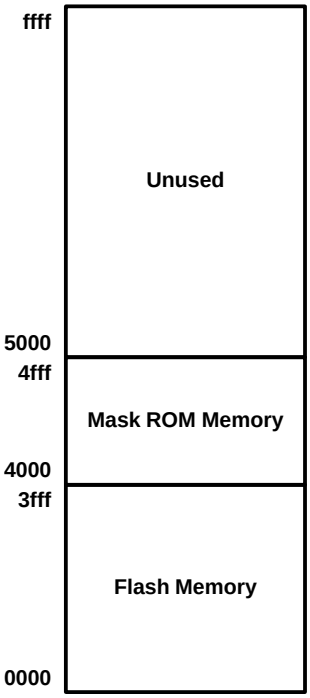


Figure 9. Program Memory Register Map

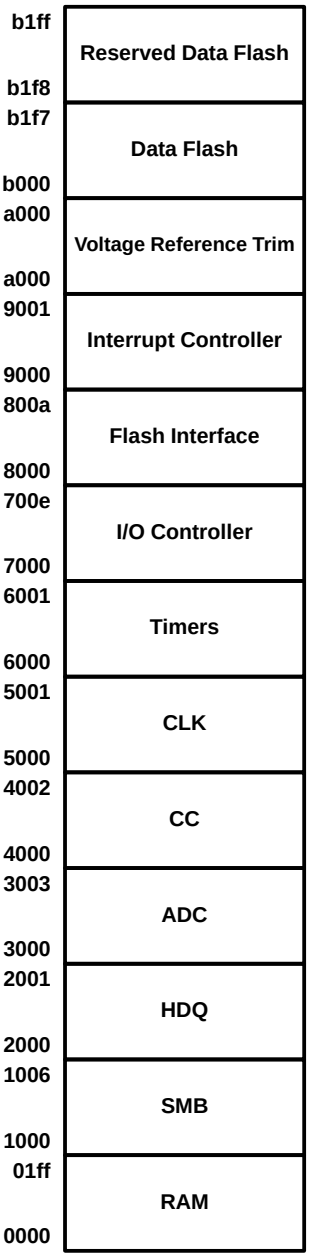


Figure 10. Data Memory Map

Table 1. bq8015 Register and Peripheral Map

Address	Symbol	Name	Read/ Write	Bit fields							
				7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
1000h	SMBMA	SMBus master mode	Write	SMBMA7	SMBMA6	SMBMA5	SMBMA4	SMBMA3	SMBMA2	SMBMA1	R/W_B
1001h	SMBDA	SMBus data	R/W	SMBD7	SMBD6	SMBD5	SMBD4	SMBD3	SMBD2	SMBD1	SMBD0
1002h	SMBACK	SMBus acknowledge	Write	—	—	—	—	—	—	—	ACK
1003h	SMBSTA	SMBus status	Read	—	D_REQ	D_RDY	SA_RDY	NACKED	BUS_FREE	UNIT_BUSY	MASTR
1004h	SMBCTL	SMBus control	R/W	—	—	BUS_LOB	PEC_DIS	BFI_EN	SMB_RST	ISOLATE	SA_EN
1005h	SMBPEC	SMBus packet error check	R/W	—	—	—	—	—	PEC_SND	PEC_CHK	PEC_VLD
1006h	SMBTAR	SMB target slave address	R/W	SMBT7	SMBT6	SMBT5	SMBT4	SMBT3	SMBT2	SMBT1	SMBT0
2000h	HDQSTA	HDQ register status	Read	—	—	—	—	HDQ_DRQ	HDQ_DRDY	SBIT_IN	DATA_IN
2001h	HDQOUT	HDQ output control register	R/W	—	—	—	—	—	—	SBIT_OUT	DATA_OUT
3000h	ADCTL0	ADC control register	R/W	CONV	VRVDD	ADC_ON	FAST	CHAN3	CHAN2	CHAN1	CHAN0
3001h	ADCTL1	ADC control register 1	Read	—	—	—	—	—	—	—	AD_DRDY
3002h	ADHI	ADC data register hi byte	Read	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
3003h	ADLO	ADC data register low byte	Read	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
4000h	CCCTL	Coulomb counter control register	R/W	—	—	—	—	—	—	CC_ON	CC_CAL
4001h	CCHI	Coulomb counter data high byte	Read	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10	CCR9	CCR8
4002h	CCLO	Coulomb counter data low byte	Read	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
5000h	CLK	Clock register	R/W	—	—	—	OSC_EN	—	PLL_OFF	LP_CLK	0
5001h	OSC_TRIM	Oscillator trim control	R/W	OTRIM7	OTRIM6	OTRIM5	OTRIM4	OTRIM3	OTRIM2	OTRIM1	OTRIM0
6000h	TMR_CTL	Timer control register	R/W	—	—	—	—	—	WDEN	WKEN	WDCRST
6001h	TIMER	Timer program register	R/W	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
7000h	RA_OUT	RA output register	R/W	RAOUT7	RAOUT6	RAOUT5	RAOUT4	RAOUT3	RAOUT2	RAOUT1	RAOUT0
7001h	RB_OUT	RB output register	R/W	RBOUT7	RBOUT6	RBOUT5	RBOUT4	RBOUT3	RBOUT2	RBOUT1	RBOUT0
7002h	RC_OUT	RC output register	R/W	RCOUT7	RCOUT6	RCOUT5	RCOUT4	RCOUT3	RCOUT2	RCOUT1	RCOUT0
7003h	RA_IN	Status of RA register inputs	Read	RAIN7	RAIN6	RAIN5	RAIN4	RAIN3	RAIN2	RAIN1	RAIN0
7004h	RB_IN	Status of RB register inputs	Read	RBIN7	RBIN6	RBIN5	RBIN4	RBIN3	RBIN2	RBIN1	RBIN0
7005h	RC_IN	Status of RC register inputs	Read	RCIN7	RCIN6	RCIN5	RCIN4	RCIN3	RCIN2	RCIN1	RCIN0
7006h	RA_IEN	Enable RA input register	R/W	RAIEN7	RAIEN6	RAIEN5	RAIEN4	RAIEN3	RAIEN2	RAIEN1	RAIEN0
7007h	RB_IEN	Enable RC input register	R/W	RBIEN7	RBIEN6	RBIEN5	RBIEN4	RBIEN3	RBIEN2	RBIEN1	RBIEN0
7008h	RC_IEN	Enable RC input register	R/W	RCIEN7	RCIEN6	RCIEN5	RCIEN4	RCIEN3	RCIEN2	RCIEN1	RCIEN0
7009h	IOCTL	IO control register	R/W	—	—	—	XEVEN	XINTEN	SMBEN	HDQEN	VOUTEN
700ah	32KOUTEN	Enable 32-kHz output	R/W	0	0	0	0	0	0	32K_OUT	0
700ch	RC_PUP	RC pullup register	R/W	RCPUP7	RCPUP6	RCPUP5	RCPUP4	RCPUP3	RCPUP2	RCPUP1	RCPUP0
9000h	PFLAG	Peripheral flag register	R/W	SMBF	HDQF	ADF	CCF	TIMF	WTF	—	—
9001h	PIE	Peripheral interrupt enable	R/W	SMBIE	HDQIE	ADIE	CCIE	TIMIE	WTIE	XINPOL	XEVPOL
a000h	VTRIM	Voltage reference trim control	R/W	—	—	—	—	VTRIM3	VTRIM2	VTRIM1	VTRIM0

system management bus (SMBus) peripheral and operation interface

The bq8015 system management bus peripheral (SMB) implements the two-wire bidirectional interface and protocol specified in the System Management Bus v1.1 specification. The SMB peripheral interfaces to the bq8015 CPU via interrupts or register polling. This peripheral can transmit and receive data as either an SMBus master or SMBus slave. The slave address for the bq8015 can be configured to respond automatically to a single slave address, or to multiple addresses if programmed into the bq8015 firmware.

The SMBus interface to the bq8015 CPU consists of seven registers and four possible types of interrupts.

SMB interrupts

D_RDY (Data Ready): This indicates that serial data have been received and are available to be read by the bq8015 CPU. This interrupt is asserted before the SMBus acknowledge clock (ACK clock is stretched).

D_REQ (Data Request): This indicates that the SMB peripheral is ready for data to be sent on the SMBus. The bq8015 CPU must supply this data via a register write. This interrupt is asserted after previous ACK clock (clock after previous ACK is stretched).

BUS_FREE: This indicates that the SMBus is not active.

SA_RDY (Slave Address Ready): This indicates that a slave address has been received and must be checked by the bq8015 CPU to determine whether the SMB peripheral acknowledges the address. While this event is not typical for SMBus peripherals, this interrupt allows the bq8015 to respond to multiple slave addresses if necessary. The interrupt occurs before ACK clock (ACK clock is stretched).

operating as a slave

Automatic acknowledgement of a slave address requires SA_EN to be set to 0 in the SMB control register (1004h). In this mode, the SMB peripheral monitors the SMBus pins, watching for the slave address programmed in SMBTAR register. When this address has been received, the SMB peripheral ACKs the address and prepare to receive the ensuing command byte. If SA_EN is set to 1, firmware is required to examine the address and determine whether to ACK the address. After this command byte has been received, D_RDY is asserted, signaling the CPU that a command has been successfully received and is available to be read from SMBDA. The CPU must then decode this command and decide whether to ACK or NACK the command by writing to the SMBACK register (1002h), clearing D_RDY. For valid commands that may be either reads or writes, the CPU cannot determine whether to prepare to send data or receive it at this point. To determine whether the command is an SMB read or write:

— If the next SMBus activity consists of a repeated start followed by the repeated target address with LSB = 1, the transaction is a slave read. The SMB ACKs the repeated address and assert D_REQ, signaling the CPU that a slave read is in progress.

— If a repeated start is not received, the SMB is prepared to continue receiving data. Upon reception of eight more bits of data, D_RDY is asserted, signaling the CPU that a slave write is in progress.

For a Slave Read:

In response to D_REQ, the CPU must write the required data to the SMBDA register (1001h), clearing D_REQ. (Note: the only way to abort the transaction at this point is to not clear D_REQ, causing the SMB to eventually time-out the SMBus and reset). Upon each succeeding assertion of D_REQ, the status of the master's ACK or NACK of the preceding transmitted byte is checked by reading the NACKED bit. Ordinarily the final data byte is NACKed by the master, indicating the master is finished receiving data. If the expected final data byte is ACKed by the master, this indicates a PEC byte is to be sent. In this case, the PEC_SND bit in the SMBPEC register (1004h) is set in response to D_REQ. This setting clears D_REQ and instruct the SMB peripheral to send a PEC byte; SMBDA should not be written. In response to the final D_REQ with NACKED = 1, the CPU should write a 0 to SMBACK to clear D_REQ.

system management bus (SMBus) peripheral and operation interface (continued)

For a Slave Write:

The SMB peripheral is receiving data sent from the master. After each byte of received data, D_RDY is asserted, signaling the CPU that the data byte is ready to be read from SMBDA. The CPU needs to ACK or NACK the byte by writing to SMBACK register, clearing D_RDY. If a data byte is to be checked as a PEC byte, the PEC_VLD bit in the SMBPEC register is checked after assertion of the final D_RDY and before writing the final ACK (or NACK).

operating as a master

The CPU must first verify that the SMBus is not currently active. Verification is by either polling the BUS_FREE bit in the SMBSTA register or setting the BFI_EN bit in the SMBCTL register. Once the bus is verified inactive, the CPU may then write the address of the slave device it wishes to communicate with to the SMBMA register. The lsb of this register is written as a 1 if the transaction is a read from the slave, otherwise the lsb is written as a 0 if the transaction is a write to the slave.

After transmitting the slave address, the SMB peripheral asserts a D_REQ. Then, successful acknowledgment of the address by the slave is indicated by the bit, NACKED = 0. If NACKED = 1, the CPU may abort the transaction by writing a 0 to SMBACK. This clears D_REQ and a stop condition is sent to free the bus. Otherwise, with NACKED = 0, the transaction is continued with the CPU writing the required SMBus command to SMBDA. This clears D_REQ and instruct the SMB peripheral to send the contents of SMBDA on the SMBus. D_REQ is asserted again after the command has been ACKed or NACKed by the slave. If ACKed, the next step is dependent on the lsb of SMBMA.

SMBMA register for an lsb = 1: (R/W_B = 1), Master Read:

D_REQ is cleared by writing a 1 to SMBACK, causing the SMB peripheral to send a repeated start followed by the repeated SLAVE address with its lsb = 1. This repeated address is ACKed or NACKed by the slave, and is verified by reading the NACKed bit after the next assertion of D_REQ. The D_REQ is cleared by writing a 1 to SMBACK. Then data are sent to the SMB peripheral from the slave device. After each byte of received data, D_RDY is asserted signaling the CPU that the data bit is ready to be read from SMBDA. The CPU then ACKs or NACKs the byte by writing to SMBACK, clearing D_RDY. If a data byte is to be checked as a PEC byte, the PEC_VLD bit is checked after assertion of the final D_RDY and before writing the final NACK. The final data byte to be read, or the PEC byte, is NACKed, which signals the SMB to end the master read and send a stop.

SMBMA register for an lsb = 0: (R/W_B = 0), Master Write:

D_REQ signals the request for data to be sent to the slave and is cleared by writing the requested data to the SMBDA register. Upon each assertion of D_REQ, the status of the slave's ACK or NACK of the preceding byte is checked by reading the NACKED bit. If a PEC byte is to be sent, PEC_SND is set in response to the D_REQ preceding the byte to be considered a PEC byte. Writing to PEC_SND clears D_REQ; the SMBDA register should not be written. If no more data is to be sent, the CPU should write a 0 to the SMBACK register in response to the final D_REQ, which clears D_REQ and send a stop.

SMB register details (address 1000h–1005h)

The following is a description of the SMBus registers.

SMBMA (address 1000h): SMBus master address register

A write to this register by the CPU initiates an SMBus master transaction, sets the desired SLAVE address and signifies the type of SMB master transaction.

SMBMA Register (Address 1000h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMBMA7	SMBMA6	SMBMA5	SMBMA4	SMBMA3	SMBMA2	SMBMA1	R/W_B
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

SMBMA7–1 (bit 7:1): The SMB address of the slave device to be accessed in master mode.

R/W_B (bit 0): SMB master-mode direction control bit. This bit controls the direction of the master-mode transaction

1 = Master–mode read transaction from slave
0 = Master–mode write transaction to slave

SMBDA (address 1001h): SMBus data register

This is the register the CPU uses to transmit data to or receive data from the SMBus where SMBD0 is the lsb and SMBD7 is the msb.

SMBDA Register (Address 1001h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMBD7	SMBD6	SMBD5	SMBD4	SMBD3	SMBD2	SMBD1	SMBD0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SMBACK (address 1002h): SMBus acknowledge register

This register is used by the CPU to ACK/NACK the previously received data, to send stop condition in master mode, or to reset the SMB engine in response to errors detected on the SMBus.

SMBACK Register (Address 1002h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	—	ACK
Access	—	—	—	—	—	—	—	W
Reset	—	—	—	—	—	—	—	0

Reserved (bits 7:1): Do not use

ACK (bit 0): acknowledge bit.

1 = Acknowledge previous data, send ACK
0 = Do not acknowledge previous data, send NACK and reset; send stop if in master mode

SMBSTA (address 1003h): SMBus status register

This read-only register reports the status of the SMBus peripheral and SMBus interface.

SMBSTA Register (Address 1003h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	D_REQ	D_RDY	SA_RDY	NACKED	BUS_FREE	UNIT_BUSY	MASTER
Access	—	R	R	R	R	R	R	W
Reset	—	0	0	0	0	0	0	0

Reserved (bit 7): Do not use.

D_REQ (bit 6): Data request bit. This bit indicates current state of D_REQ interrupt.

1 = D_REQ asserted
0 = D_REQ not asserted

D_RDY (bit 5): Data ready bit. This bit indicates current state of D_RDY interrupt.

1 = D_RDY asserted
0 = D_RDY not asserted

SA_RDY (bit 4): Slave address ready bit. This bit indicates current state of SA_RDY interrupt.

1 = SA_RDY asserted
0 = SA_RDY not asserted

NACKED (bit 3): Not acknowledged bit. This bit indicates state of previously sent data's acknowledgment by the destination device (also indicates lost arbitration as a master).

1 = Previous data NACKed, or SMB has lost arbitration while operating as a master
0 = Previous data successfully ACKed

BUS_FREE (bit 2): Bus free bit. This bit indicates active state of the SMBus.

1 = SMBus inactive
0 = Activity detected on the SMBus

UNIT_BUSY (bit 1): SMB peripheral busy bit. This bit indicates active state of SMB engine.

1 = SMB engine processing an SMBus transaction as either a master or slave
0 = SMB engine idle

MASTER (bit 0): Master bit. This bit indicates whether or not the SMB engine is currently operating as an SMBus master.

1 = SMB engine has successfully attained master mode
0 = SMB engine is not currently operating as an SMBus master

SMBCTL (address 1004h): SMBus control register

This read-write register controls the operation of the SMBus peripheral.

SMBCTL Register (Address 1004h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	BUSLOB	PEC_DIS	BFI_EN	SMB_RST	ISOLATE	SA_EN
Access	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Reset	—	—	0	0	0	0	0	0

Reserved (bits 7:6): Do not use.

BUSLOB (bit 5): Bus low detection bit. This bit is used to determine if the SMBus clock and data lines have both been low for more than two seconds. This bit is used to implement the charger broadcast re-enable function as described in the Smart Battery Data specification. BUSLOB must be written back to a logic one by the user before another BUSLOB event can be detected.

1 = SMBus clock and data have not been low for over two seconds after written to a logic one
0 = SMBus clock and data have been low for over two seconds

PEC_DIS (bit 4): Packet error checking engine disable bit. This bit disables PEC engine to conserve power if PEC checking or generation is not required.

1 = PEC engine disabled
0 = PEC engine enabled

BFI_EN (bit 3): Bus free interrupt enable bit. This bit enables interrupt when BUS_FREE is set.

1 = Assert interrupt in response to BUS_FREE assertion
0 = Mask assertion of interrupt in response to BUS_FREE assertion; BUS_FREE must be polled to determine active state of SMBus

SMB_RST (bit 2): SMB engine software reset bit.

1 = Reset SMB engine
0 = SMB normal operation

ISOLATE (bit 1): SMBus isolation bit. This bit isolates SMB peripheral from SMBus.

1= Disconnect SMB peripheral from SMBus
0 = SMB normal operation

SA_EN (bit 0): Slave address detection enable bit. This bit enables assertion of SA_RDY to allow the device to respond to multiple slave addresses.

1 = SA_RDY asserted in response to any slave address detected on SMBus; CPU required to ACK or NACK address via SMBACK
0 = SMB normal operation; SMB engine ACKs address programmed in SMBTAR without CPU intervention

SMBPEC (address 1005h): SMBus Packet Error Check Register

This register manages the PEC generation and control for SMBus transactions.

SMBPEC Register (Address 1005h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	PEC_SND	PEC_CHK	PEC_VLD
Access	—	—	—	—	—	R/W	R/W	R/W
Reset	—	—	—	—	—	0	0	0

Reserved (bits 7:3): Do not use.

PEC_SND (bit 2): PEC send bit. This bit instructs SMB engine to send calculated PEC byte of previously transmitted SMBus data; it is set in response to a DATA_REQ assertion.

1 = Send PEC byte (cleared by hardware)
0 = Do not send PEC byte

PEC_CHK (bit 1): PEC check bit. This bit instructs SMB engine to expect calculated PEC byte of previously transmitted SMBus data, or successful nonPEC termination of proceeding transaction; it is set in response to a D_RDY assertion.

1 = Check PEC byte (cleared by hardware)
0 = Do not check PEC byte

PEC_VLD (bit 0): PEC valid bit. This bit indicates validity of previously received PEC byte or successful nonPEC termination of previous SMBus transaction; it is read only in response to a D_RDY assertion.

1 = PEC byte was valid or a valid stop was received for a nonPEC transaction
0 = PEC byte was not valid

SMBTAR (address 1006h): SMBus target slave register

This register contains the slave address that the SMB engine responds to where SMT0 is the lsb and SMT7 is the msb.

SMBTAR Register (Address 1006h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMT7	SMT6	SMT5	SMT4	SMT3	SMT2	SMT1	SMT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

HDQ single-pin serial interface peripheral

The HDQ serial interface peripheral may be used to implement a single-wire serial interface. For flexibility, the HDQ peripheral performs all bit-framing for the transmission and reception of data and BREAK signals. Since this peripheral is a bit engine, all command and data formatting is a function of the user firmware offering maximum flexibility. The user firmware is required to format the received bits in a timely fashion and to transmit data bits out in the correct cycle time and format. The engine may be set up for interrupt driven operation, or polling may be used to determine peripheral status.

The HDQ interface is an asynchronous return-to-one protocol where a processor sends the command code to the bq8015. With HDQ, the least significant bit (lsb) of a data byte (command) or word (data) is transmitted first. Note that the RA5/HDQ pin is open drain and requires an external pullup resistor. The 8-bit command code consists of two fields, the 7-bit HDQ command code (bits 0–6) and the 1-bit R/W field (msb bit 7). The R/W field directs the bq8015 either to

- Store the next 8 or 16 bits of data to a specified register or
- Output 8 or 16 bits of data from the specified register

The HDQ peripheral can transmit and receive data as either an HDQ master or slave.

The return-to-one data bit frame of HDQ consists of three distinct sections. The first section is used to start the transmission by either the host or by the bq8015 taking the HDQ pin to a logic-low state for a time $t_{STRH,B}$. The next section is for data transmission, where the data are valid for a time t_{DSU}, after the negative edge used to start communication. The data are held until a time t_{DV}, allowing the host or bq8015 time to sample the data bit. The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a time t_{SSU}, after the negative edge used to start communication. The final logic-high state is held until the end of $t_{CYCH,B}$, allowing time to ensure the transmission was stopped correctly. The timing for data and break communication are given in the HDQ characteristics section.

HDQ serial communication is normally initiated by the host processor sending a break command to the bq8015. A break is detected when the HDQ pin is driven to a logic-low state for a time t_B or greater. The HDQ pin should then be returned to its normal ready high logic state for a time t_{BR}. The bq8015 is now ready to receive information from the host processor.

The HDQ peripheral is enabled by setting HDQEN=1 in the IOCTL register. HDQIE (bit 6 of the PIE register) and GIE (bit 5 of the internal CPU status register) must be set to a logic one for HDQ interrupt processing occur (address vector (3h)). Refer to the interrupt processing section for more information about setting HDQIE and GIE. An HDQ interrupt (HDQF=HDQIE=GIE=1) is generated by the receiving valid data, a break condition or when the HDQ engine has finished transmitting and is ready to accept more data for transmission.

Data bits transmitted to the bq8015 are read via the HDQSTA register. The HDQ_DRDY bit is asserted by incoming data. Valid data are assumed when HDQ_DRDY=SBIT_IN=1. The data bit, DATA_IN, is stored allowing further command or data processing by the bq8015. When HDQ_DRDY=1 and SBIT_IN=0, a BREAK or communication collision is assumed and the communication process restarted.

Data bits are output via the HDQOUT register. The first bit in a transmission may be sent by writing the appropriate data and stop bit to the DATA_OUT and SBIT_OUT bits, respectively. Subsequent data are sent after HDQ_DREQ is asserted signifying that the transmission of the previous data is complete. A BREAK is transmitted by writing DATA_OUT=SBIT_OUT=0.

HDQSTA (address 2000h): HDQ input and interrupt control register

This register manages the HDQ interface and control status.

HDQSTA Register (Address 2000h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	HDQ_DRQ	HDQ_DRDY	SBIT_IN	DATA_IN
Access	—	—	—	—	R	R	R	R
Reset	—	—	—	—	—	—	—	—

Reserved (bit 7:4): Do not use.

HDQ_DRQ (bit 3): HDQ data request bit. Indicates current state of HDQ_DREQ interrupt; automatically cleared when read

1 = HDQ_DREQ asserted
0 = HDQ_DREQ not asserted

HDQ_DRDY (bit 2): HDQ data request ready bit. Indicates current state of HDQ_DRDY interrupt; automatically cleared when read

1 = HDQ_DRDY asserted
0 = HDQ_DRDY not asserted

SBIT_IN (bit 1): HDQ stop bit In. Value of stop bit read from HDQ

1 = Stop bit equals 1
0 = Stop bit equals 0 (a break was received if DATA_IN=0)

DATA_IN (bit 0): HDQ data in. Value of data bit read from HDQ

1 = HDQ data in equals 1
0 = HDQ data in equals 0

HDQOUT (address 2001h): HDQ output control register

This register manages the HDQ output control.

HDQOUT Register (Address 2001h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	SBIT_OUT	DATA_OUT
Access	—	—	—	—	—	—	R/W	W
Reset	—	—	—	—	—	—	—	—

Reserved (bits 7:2): Do not use.

SBIT_OUT (**bit 1):** HDQ stop bit out value of stop bit to be transmitted on bus

1 = Send a stop bit of 1
0 = Send a stop bit of 0 (sends a break if DATA_OUT=0)

DATA_OUT (bit 0): HDQ data out. Value of data bit to be transmitted on bus

1 = Send a 1
0 = Send a 0

analog-to-digital converter (ADC) operation

The ADC peripheral on the bq8015 consists of an analog multiplexer and a delta-sigma converter. The multiplexer can be configured to connect one of twelve different signals to the converter. For low-power operating modes, the ADC can be turned off under software control. Typical operation requires only a single write to the ADCTL0 register to simultaneously configure the ADC and issue a convert command. Configuring the ADC includes enabling the peripheral (ADC_ON) and selecting the desired voltage referenced (VRVDD), filter length (FAST), and multiplexer channel (CHAN3:CHAN0). The conversion starts on the rising edge of CONV. CONV must be held high until the conversion is complete and data has been read from ADLO and ADHI. The ADC_DRDY bit (bit 0 in ADCTL1 register) is asserted upon completion of a conversion to signal that valid data are available in the ADLO and ADHI registers. The ADF flag bit in the PFLAG register is also asserted when ADC_DRDY goes to a one. An interrupt may be generated on the rising edge of ADC_DRDY; see the Interrupt Control Section for details.

CONV must be set to a zero before performing additional conversions. This clears ADC_DRDY ADLO, and ADHI and reset the converter. Once CONV is set to zero, the converter is ready to perform additional conversions or for the setup to change. The data in ADHI–ADLO are stored in 2s complement format. Full scale (7FFFh) is referred to the reference voltage, Vref, typically 1.225 V using the internal reference or VDD using the external reference. The least significant bit (lsb) for a single conversion is 37.38 μV when the internal reference is used. When FAST=1, even though the effective number of bits is 10, a 16-bit result is still provided. Better resolution can be obtained by averaging this 16-bit result.

NOTE:

For the specified accuracy, the ADC input range is limited to 80% of the ADC reference input, either VDD or internal Vref.

ADCTLO (address 3000h): ADC Control register

This is one of the ADC peripheral control registers.

ADCTL0 Register (Address 3000h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CONV	VRVDD	ADC_ON	FAST	CHAN3	CHAN2	CHAN1	CHAN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CONV (bit 7): Convert command bit. This bit is used to start a conversion.

1 = Conversion started on the rising edge of CONV; CONV is held high until after valid data have been read from ADLO and ADHI (ADC_DRDY =1)
0 = ADC held in reset; ADC_DRDY =0 and ADLO = 00h, ADHI = 80h

VRVDD (bit 6): Voltage reference selection bit. This bit selects which voltage reference (either VDD or internal VREF) is used by the ADC.

1 = Selects VDD as the ADC reference voltage for ratiometric conversions
0 = Selects the internal VREF as the ADC reference voltage

ADC_ON (bit 5): ADC power control bit. This bit powers the ADC and the multiplexer.

1 = ADC power is on
0 = ADC power off and the multiplexer input impedance high

FAST (bit 4): Filter length selection bit. This bit selects between the 512 or 8192 length digital filter.

1 = 512 length decimation filter. Conversion time is 1.95 ms.
0 = 8192 length decimation filter. Conversion time is 31.25 ms.

ADCTLO (address 3000h): ADC Control register (continued)

CHAN3–CHAN0 (bit 3–0): Channel selection bits. These bits select which of twelve multiplexer inputs is converted.

CHAN3–CHAN0	ADC INPUT CHANNEL
0000	RC0
0001	RC1
0010	RC2
0011	RC3
0100	RC4
0101	RC5
0110	RC6
0111	RC7
1000	DSCP
1001	DSCM
1010	VTEMP
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	VSSA

ADCTL1 (address 3001h): ADC control register 1

This register signals when data is ready from the ADC peripheral.

ADCTL1 Register (Address 3001h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	—	ADC_DRDY
Access	—	—	—	—	—	—	—	R
Reset	1	0	0	0	0	0	0	0

Reserved (bits 7:1): Do not use.

ADC_DRDY (bit 0): Data ready flag. This read-only bit signals when valid data are ready in ADLO and ADHI.

1 = Valid data are ready
0 = Conversion in progress or ADC held in reset, ADC_DRDY goes low on the falling edge of CONV

ADLO, ADHI (address 3003h, 3002h): ADC data registers

These store the result of the ADC data after conversion is complete. ADR0 is the lsb and ADR15 is the msb.

ADHI Register (Address 3002h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
Access	R	R	R	R	R	R	R	R
Reset	0	1	0	0	0	0	0	0

ADL0 Register (Address 3003h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

coulomb counter operation

The coulomb counter peripheral is a single-channel over-sampled converter with continuous sampling and is optimized for tracking charge and discharge activity of a rechargeable battery. The coulomb counter (CC) in normal operation is configured to convert the differential voltage across pins DSCP and DSCM. The coulomb counter design allows the integration of successive samples with no loss or corruption of data. This integration further reduces quantization error over time, thereby increasing system resolution. The coulomb counter can be turned on or off under firmware control, enabling greater power efficiency.

Coulomb counting is accomplished by integrating the voltage across a sense resistor placed in series with the negative terminal of a battery. After a power-on reset, the default state of the CC peripheral is off. The CC peripheral is enabled by setting the CC_ON bit to one in the CCCTL register. The CC inputs, DSCP and DSCM, are configured for normal operation by writing CC_CAL to a zero in the CCCTL register. The conversions begins automatically after CC_ON is set to a one. The converter asserts the CCF flag bit in the PFLAGS register once every 250 ms. An interrupt is generated when CCF is set, assuming CCIE = PIE = GIE = 1. CCLO and CCHI are then read and CCF cleared before another 250 ms have elapsed, avoiding corruption or data loss when the registers are updated following the next conversion.

The data in CCHI–CCLO are stored in 2s complement format where full scale (7FFFh) is referred to V_{ref}, typically 1.225 V. The allowable voltage range for DSCP and DSCM is –0.3V to 1.0 V. The differential voltage between DSCP and DSCM are limited to less than 1.0 V. The least significant bit (lsb) for a single conversion is 37.38 μV or 2.60 nVh. The charge lsb can be determined by dividing 2.60 nVh by the value of the sense resistor. Resolution is improved by summing (integrating) consecutive samples since no information is lost between conversions.

Calibration cycles can be performed at any time. If the coulomb counter is off, set CC_CAL and CC_ON to one. If the coulomb counter is on and the conversion result is desired, wait until the conversion is complete and then read the data in CCLO and CCHI. After the data are read, turn the coulomb counter off by writing CC_ON to zero. This ensures that the converter is reset, and calibration can then be performed by setting CC_CAL and CC_ON to one. If the coulomb counter is on and the conversion result is not wanted, simply turn off the coulomb counter by writing CC_ON to zero. Calibration can then be performed by setting CC_CAL and CC_ON to one. Averaging of successive conversion results improves the offset resolution and better cancels the offset. One of several offset cancellation algorithms may be chosen, depending upon the required performance and operating conditions.

After exiting sleep mode, it is not necessary to wait for the PLL frequency to settle, to start a coulomb-counter conversion. A conversion can start immediately after waking from sleep. For dc inputs, a conversion error less than one LSB can be achieved. However, if greater accuracy is required, wait until the PLL settles before initiating a conversion. When a conversion starts while the PLL is settling, the conversion time is slightly longer than 250ms.

To save power, turn the converter off by setting CC_ON to a logic zero.

coulomb counter operation (continued)

CCCTL (address 4000h): coulomb counter control register

This register controls the CC peripheral.

CCCTL Register (Address 4000h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	CC_ON	CC_CAL
Access	—	—	—	—	—	—	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Reserved (bits 7:2): Do not use.

CC_ON (bit1): Coulomb counter enable. This bit enables power to the coulomb counter peripheral.

1 = Coulomb counter power turned on
0 = Coulomb counter power turned off and DSCP and DSCM inputs are high-impedance state

CC_CAL (bit0): Coulomb counter calibration input control bit. This bit controls the differential input to the coulomb counter.

1 = Both inputs to the coulomb counter driven from DSCM for calibration
0 = Coulomb counter inputs driven differentially from pins DSCP and DSCM for normal operation

CCLO, CCHI (address 4002h, 4001h): coulomb counter data register

Coulomb counter register pair stores the result of the coulomb counter operation in two 8-bit registers, CCLO and CCHI, in 2s complement format where CCR0 is the lsb and CCR15 is the msb.

CCLO Register (Address 4002h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

CCHI Register (Address 4001h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10	CCR9	CCR8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

PLL clock generator peripheral

The PLL clock generator peripheral contains all of the necessary circuitry to generate the internal clocks for the bq8015. The peripheral is composed of an internal oscillator, Phase-locked-loop (PLL), and nonoverlapping clock circuit. The nominal clock frequency used by the bq8015 is 4.194 MHz, while the analog circuitry is clocked at 262.144 kHz. The peripheral also provides a 1.049-MHz clock for the SMB engine and a 32.768-kHz clock for the internal timers.

The bq8015 requires an external 100 kΩ resistor to bias the internal oscillator. Since the temperature drift of this resistor directly affects the drift of the oscillator frequency, a low temperature drift resistor is required. The CLK register control bits reset during a POR or MRST. During a POR or MRST, the clock peripheral enters a low-power state, and after the reset the clock control bits are set to ensure that the clock is enabled. A watchdog reset is treated differently. If a watchdog reset occurs, the PLL_OFF and LP_CLK bits are set to logic zeros. A watchdog reset does not affect the OSC_EN control bit.

PLL clock generator peripheral (continued)

NOTE:

LP_CLK is recommended only for entering hibernate and sleep modes. The device may fail if LP_CLK is enabled for normal operation. After enabling LP_CLK, the CPU should be halted using only the *or stat, #mask* and *halt* instructions. For example the only instructions executed after enabling LP_CLK are the following:

```
or stat, #GIE
halt
```

To enter sleep, 0x16 is written to address 0x5000. This enables LP_CLK and turns off the PLL. To enter hibernate, 0x06 is written to address 0x5000. When entering hibernate, in addition to enabling LP_CLK and turning off the PLL, the internal oscillator is powered off. In order to prevent the device from hanging after the register is written, the internal oscillator is not actually powered off until a halt instruction is executed.

Because the CPU is halted, waking from sleep is accomplished by communication on the HDQ or SMB pins, an external event or interrupt, or an internal interrupt. Since all of the clocks on the device are off during hibernate, external pins are the only available means to enable the clocks. Specifically, the HDQ, SMBC, SMBD, EV, and INT pins can be used to power up both the oscillator and PLL. If there is an external event or interrupt, or if there is communication on the HDQ or SMB pins, the oscillator and PLL powers up again and LP_CLK goes low.

When the device is waking from sleep, or hibernate during the first 4 ms (if there is a valid SMB start condition), the SMBus holds the SMB clock line low until the PLL frequency stabilizes. By 4 mS after the PLL is enabled, the frequency is stable and SMB communication can occur

The PLL requires the addition of an external loop filter. The components are a 62 kΩ resistor in series with a 2.2-nF capacitor, the series combination is shunted by a 150 pF capacitor.

When the PLL is powered off, the bq8015 requires approximately 1.5 ms to 4 ms to stabilize the PLL when it is re-enabled.

The internal oscillator is trimed at the factory using the OSC_TRIM register (5001b). The factory determined OSC_TRIM value is loaded when the bq8015 powers up. Changing the value of OSC_TRIM may cause the device to fail.

PLL clock generator peripheral (continued)

CLK (address 5000h): clock register

This register contains the clock configuration bits for the bq8015.

CLK Register (Address 5000h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	OSC_EN	—	PLL_OFF	LP_CLK	—
Access	—	—	—	R/W	—	R/W	R/W	—
During POR/MRST	0	0	0	0	1	1	0	0
After POR/MRST	0	0	0	1	0	0	0	0
During and After WDRST	—	—	—	Prior state	Prior state	0	0	0
WAKE	0	0	0	1	Prior state	0	0	0

Reserved (bits 7:5): Do not use.

Reserved (bit 3): Do not use.

Reserved (bit 0): Must be written to 0 for proper device operation.

OSC_EN (bit 4): Internal oscillator enable. This bit powers up the internal oscillator circuitry.

1 = Oscillator on
0 = Oscillator off when a halt is issued by the microprocessor

PLL_OFF (bit 2): PLL power control. This bit disables and enables power to the PLL. This signal is also used to control power to the bias circuitry. When the PLL is enabled, it takes 3.9 ms until the 1.049-MHz clock is available assuming that the crystal oscillator has been on.

1 = PLL off.
0 = PLL on.

LP_CLK (bit 1): Lower power clock control. This bit controls the CPU clock frequency and is recommended only when entering low-power, sleep, or hibernate modes.

1 = CPU clock frequency 32.768 kHz
0 = CPU clock frequency 4.194 MHz

OSC_TRIM (address 5001h): oscillator trim register

This register contains the oscillator trim register bits for the bq8015.

OSC_TRIM Register (Address 5001h)								
Name	**OTRIM7**	**OTRIM6**	**OTRIM5**	**OTRIM4**	**OTRIM3**	**OTRIM2**	**OTRIM1**	**OTRIM0**
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

OTRIM 7:0 (bits 7:0): Trim values used to calibrate the internal oscillator.

timers description

The bq8015 has three internal timers: an interrupt timer, a bus-low timer, and a watchdog timer. The internal oscillator operates the three timers, so if the oscillator is disabled, these timers do not function.

The interrupt timer is free-running and has a period of 7.8125 ms. When the TIMIE bit (bit 3) is enabled in the PIE register, the interrupt controller requests interrupt servicing at every interrupt timer clock period. The bus-low timer is also free running and is used in conjunction with bus-monitoring circuitry to determine if the battery has been removed from the system for more than two seconds. The sample period of the bus-low timer is 125 ms. The interrupt timer and the bus-low timer are reset by any reset event (POR, MRST, or watchdog reset).

The watchdog timer provides a periodic system reset unless it is cleared by the processor. The interval between resets is programmable. The watchdog timer can also be programmed to provide a wake signal, which is a processor event. Clearing the watchdog timer clears both the watchdog-reset signal and the wake signal. The timer program register sets the period of the wake signal. The period of the watchdog-reset signal is then set to twice the wake period. The timer control and program registers are only reset by the POR and MRST. The watchdog reset has no effect on these registers.

TMR_CTL (address 6000h): timer control register

TMR_CNTL Register (Address 6000h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	WDEN	WKEN	WDCRST
Access	—	—	—	—	—	R/W	R/W	R/W
During POR/MRST	0	0	0	0	0	0	0	1
After POR/MRST	0	0	0	0	0	0	0	0

Reserved (bits 7:3): Do not use.

WDEN (bit 2): Watchdog enable. This bit enables the watchdog reset signal.

1 = Watchdog reset enabled
0 = Watchdog reset disabled

WKEN (bit 1): Wake enable. This bit enables the wake timer.

1 = The timer issues a wake signal.
0 = No wake signal is provided.

WDCRST (bit 0): Watchdog counter reset. This bit resets the watchdog counter and must be set periodically by the processor in order to avoid a watchdog reset. This register bit is cleared by the watchdog circuitry after the internal watchdog counter is reset. This bit also clears the wake counter.

1 = The watchdog counter is reset.
0 = Watchdog counting if enabled

If the bq8015 enters hibernation mode (the internal oscillator is stopped), the registers keep their values throughout hibernation and remain in this state when the bq8015 exits hibernation. If WDEN is high, the watchdog counter stops when the crystal oscillator is stopped. It resumes counting from the previous point when the oscillator starts again.

TIMER (address 6001h): timer program register

The timer program register sets the wake and watchdog reset period. The minimum wake period is 3.90625 ms when the register is set to 00h. The maximum wake period is one second when the program register is set to FFh. The program register allows the user to program the period between the minimum and maximum values in 3.90625 ms steps. The program register also sets the watchdog reset period to twice the wake period. Therefore, the minimum watchdog reset period is 7.8125 ms and the maximum reset period is two seconds. The programming step size is 7.8125 ms.

Since both the wake signal and watchdog reset are operated from the same counter, care must be used when enabling each signal. Enabling one signal while the other signal is already enabled does not reset the state of the counter. To ensure proper timing, in this situation the user should clear the counter before enabling the second signal. Clearing can be accomplished by writing 0 to both WDEN and WKEN bits in the TMR_CNTL register followed by setting the enable bits to 1.

TIMER Register (Address 6001h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
During POR/MRST	1	1	1	1	1	1	1	1

The timer register is programmed where TP0 is the lsb and TP7 is the msb.

I/O pin controller

The I/O controller manages the operation of the three general-purpose, eight-bit data ports on the bq8015. These three ports, pins RA[7:0], RB[7:0] and RC[7:0] can function independently as digital input pins, digital open-drain output pins, or both. In addition, the pins of the RC port can be selected as analog inputs to the analog-to-digital converter peripheral (ADC) and can be programmed to enable internal pullups to provide full push-pull digital output functionality.

Several of the RA and RB pins have predefined functionality providing communication interfaces for the two bq8015 serial communication peripherals, and providing external interrupt/event conditions to the onboard processor. The predefined functions can be disabled based upon the user program. The predefined pins are:

RA7 – SMBus data pin
RA6 – SMBus clock pin
RA5 – HDQ serial communication pin
RA1 – VOUT pin (voltage supply output)
RB1 – external event pin
RB0 – external interrupt pin

NOTE:

Attempting to use RA7, RA6 or RA5 as general-purpose I/O pins while the SMB or HDQ peripherals are enabled could produce undesired behavior. Therefore, the SMB or HDQ functionality is disabled via the IOCTL register before using these pins as general-purpose data pins. Likewise, the external interrupt/event conditions are disabled to prevent unintended interrupt/event conditions if RB1 or RB0 are to be used for general-purpose I/O.

Pin RA1 contains an internal pullup for use as an external power source controlled by the VOUT bit.

RA_OUT (address 7000h): RA output register

The RA output register controls the output state of the RA pins.

RA_OUT Register (Address 7000h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RAOUT7	RAOUT6	RAOUT5	RAOUT4	RAOUT3	RAOUT2	RAOUT1/VOUT	RAOUT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

RAOUT7 (bit 7): 1 = Do not drive pin RA7 (open drain 3-state); required state for using SMBD
0 = Drive pin RA7 to a logic 0

RAOUT6 (bit 6): 1 = Do not drive pin RA6 (open drain 3-state); required state for using SMBC
0 = Drive pin RA6 to a logic 0

RAOUT5 (bit 5): 1 = Do not drive pin RA5 (open drain 3-state); required state for using HDQ
0 = Drive pin RA5 to a logic 0

RAOUT4 (bit 4): 1 = Do not drive pin RA4 (open drain 3-state)
0 = Drive pin RA4 to a logic 0

RAOUT3 (bit 3): 1 = Do not drive pin RA3 (open drain 3-state)
0 = Drive pin RA3 to a logic 0

RAOUT2 (bit 2): 1 = Do not drive pin RA2 (open drain 3-state)
0 = Drive pin RA2 to a logic 0

RAOUT1 (bit 1): 1 = Drive pin RA1/VOUT to a logic 1 if VOUTEN=1; otherwise, RA1 is open-drain 3-state
0 = Drive pin RA1/VOUT to a logic 0

RAOUT0 (bit 0): 1 = Do not drive pin RA0 (open drain 3-state)
0 = Drive pin RA0 to a logic 0

RB_OUT (address 7001h): RB output register

The RB output register controls the output state of the RB pins.

RB_OUT Register (Address 7001h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RBOUT7	RBOUT6	RBOUT5	RBOUT4	RBOUT3	RBOUT2	RBOUT1	RBOUT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

RBOUT7 (bit 7): 1 = Do not drive pin RB7 (open drain 3-state)
0 = Drive pin RB7 to a logic 0

RBOUT6 (bit 6): 1 = Do not drive pin RB6 (open drain 3-state)
0 = Drive pin RB6 to a logic 0

RBOUT5 (bit 5): 1 = Do not drive pin RB5 (open drain 3-state)
0 = Drive pin RB5 to a logic 0

RBOUT4 (bit 4): 1 = Do not drive pin RB4 (open drain 3-state)
0 = Drive pin RB4 to a logic 0

RBOUT3 (bit 3): 1 = Do not drive pin RB3 (open drain 3-state)
0 = Drive pin RB3 to a logic 0

RBOUT2 (bit 2): 1 = Do not drive pin RB2 (open drain 3-state)
0 = Drive pin RB2 to a logic 0

RBOUT1 (bit1): 1 = Drive pin RB1 (open drain 3-state) required state for using EV
0 = Drive pin RB1 to a logic 0

RBOUT0 (bit 0): 1 = Drive pin RB0 (open drain 3-state) required state for using INT
0 = Drive pin RB0 to a logic 0

RC_OUT (address 7002h): RC output register

This register controls the state of the RC pins.

RC_OUT Register (Address 7002h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RCOUT7	RCOUT6	RCOUT5	RCOUT4	RCOUT3	RCOUT2	RCOUT1	RCOUT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

RCOUT7 (bit 7): 1 = If RCPUP0=1, drive pin RC7 to a logic 1. If RCPUP0=0, do not drive pin RC7 (open drain 3-state)
0 = Drive pin RC7 to a logic 0

RCOUT6 (bit 6): 1 = If RCPUP0=1, drive pin RC6 to a logic 1. If RCPUP0=0, do not drive pin RC6 (open drain 3-state)
0 = Drive pin RC6 to a logic 0

RCOUT5 (bit 5): 1 = If RCPUP0=1, drive pin RC5 to a logic 1. If RCPUP0=0, do not drive pin RC5 (open drain 3-state)
0 = Drive pin RC5 to a logic 0

RCOUT4 (bit 4): 1 = If RCPUP0=1, drive pin RC4 to a logic 1. If RCPUP0=0, do not drive pin RC4 (open drain 3-state)
0 = Drive pin RC4 to a logic 0

RCOUT3 (bit 3): 1 = If RCPUP0=1, drive pin RC3 to a logic 1. If RCPUP0=0, do not drive pin RC3 (open drain 3-state)
0 = Drive pin RC3 to a logic 0

RCOUT2 (bit 2): 1 = If RCPUP0=1, drive pin RC2 to a logic 1. If RCPUP0=0, do not drive pin RC2 (open drain 3-state)
0 = Drive pin RC2 to a logic 0

RCOUT1 (bit 1): 1 = If RCPUP0=1, drive pin RC1 to a logic 1. If RCPUP0=0, do not drive pin RC1 (open drain 3-state)
0 = Drive pin RC1 to a logic 0

RCOUT0 (bit 0): 1 = If RCPUP0=1, drive pin RC0 to a logic 1 if RCPUP0=0, do not drive pin RC0 (open drain 3-state)
0 = Drive pin RC0 to a logic 0

RA_IN (address 7003h): RA input status register

This register determines the input state of the RA pins.

RA_IN Register (Address 7003h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RAIN7	RAIN6	RAIN5	RAIN4	RAIN3	RAIN2	RAIN1	RAIN0
Access	Read	Read	Read	Read	Read	Read	Read	Read
Reset	0	0	0	0	0	0	0	0

RAIN7 (bit 7): 1 = Logic value being driven on pin RA7 if RAIEN7=1
0 = Logic 0 value being driven on pin RA7

RAIN6 (bit 6): 1 = Logic value being driven on pin RA6 if RAIEN6=1
0 = Logic 0 value being driven on pin RA6

RAIN5 (bit 5): 1 = Logic value being driven on pin RA5 if RAIEN5=1
0 = Logic 0 value being driven on pin RA5

RAIN4 (bit 4): 1 = Logic value being driven on pin RA4 if RAIEN4=1
0 = Logic 0 value being driven on pin RA4

RAIN3 (bit 3): 1 = Logic value being driven on pin RA3 if RAIEN3=1
0 = Logic 0 value being driven on pin RA3

RAIN2 (bit 2): 1 = Logic value being driven on pin RA2 if RAIEN2=1
0 = Logic 0 value being driven on pin RA2

RAIN1 (bit 1): 1 = Logic value being driven on pin RA1 if RAIEN1=1
0 = Logic 0 value being driven on pin RA1

RAIN0 (bit 0): 1 = Logic value being driven on pin RA0 if RAIEN0=1
0 = Logic 0 value being driven on pin RA0

RB_IN (address 7004h): RB input status register

This register determines the state of the RB pins.

RB_IN Register (Address 7004h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RBIN7	RBIN6	RBIN5	RBIN4	RBIN3	RBIN2	RBIN1	RBIN0
Access	Read	Read	Read	Read	Read	Read	Read	Read
Reset	0	0	0	0	0	0	0	0

RBIN7 (bit 7): 1 = Logic value being driven on pin RB7 if RBIEN7=1
0 = Logic 0 value being driven on pin RBN7

RBIN6 (bit 6): 1 = Logic value being driven on pin RB6 if RBIEN6=1
0 = Logic 0 value being driven on pin RBN6

RBIN5 (bit 5): 1 = Logic value being driven on pin RB5 if RBIEN5=1
0 = Logic 0 value being driven on pin RBN5

RBIN4 (bit 4): 1 = Logic value being driven on pin RB4 if RBIEN4=1
0 = Logic 0 value being driven on pin RBN4

RBIN3 (bit 3): 1 = Logic value being driven on pin RB3 if RBIEN3=1
0 = Logic 0 value being driven on pin RBN3

RBIN2 (bit 2): 1 = Logic value being driven on pin RB2 if RBIEN2=1
0 = Logic 0 value being driven on pin RBN2

RBIN1 (bit 1): 1 = Logic value being driven on pin RB1 if RBIEN1=1
0 = Logic 0 value being driven on pin RBN1

RBIN0 (bit 0): 1 = Logic value being driven on pin RB0 if RBIEN0=1
0 = Logic 0 value being driven on pin RBN0

RC_IN (address 7005h): RC input status register

This register determines the state of the RC pins.

RC_IN Register (Address 7005h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RCIN7	RCIN6	RCIN5	RCIN4	RCIN3	RCIN2	RCIN1	RCIN0
Access	Read	Read	Read	Read	Read	Read	Read	Read
Reset	0	0	0	0	0	0	0	0

RCIN7 (bit 7): 1 = Logic value being driven on pin RC7 if RCIEN7=1
0 = Logic 0 value being driven on pin RCN7

RCIN6 (bit 6): 1 = Logic value being driven on pin RC6 if RCIEN6=1
0 = Logic 0 value being driven on pin RCN6

RCIN5 (bit 5): 1 = Logic value being driven on pin RC5 if RCIEN5=1
0 = Logic 0 value being driven on pin RCN5

RCIN4 (bit 4): 1 = Logic value being driven on pin RC4 if RCIEN4=1
0 = Logic 0 value being driven on pin RCN4

RCIN3 (bit 3): 1 = Logic value being driven on pin RC3 if RCIEN3=1
0 = Logic 0 value being driven on pin RCN3

RCIN2 (bit 2): 1 = Logic value being driven on pin RC2 if RCIEN2=1
0 = Logic 0 value being driven on pin RCN2

RCIN1 (bit 1): 1 = Logic value being driven on pin RC1 if RCIEN1=1
0 = Logic 0 value being driven on pin RCN1

RCIN0 (bit 0): 1 = Logic value being driven on pin RC0 if RCIEN0=1
0 = Logic 0 value being driven on pin RCN0

RA_IEN (address 7006h): RA input enable register

This register enables the RA register as an input.

RA_IEN Register (Address 7006h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RAIEN7	RAIEN6	RAIEN5	RAIEN4	RAIEN3	RAIEN2	RAIEN1	RAIEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RAIEN6 (bit 6): 1 = Enable reading of logic value on pin RA7 via RAIN7
0 = Disable reading of logic value and guard against floating input levels on pin RA7

RAIEN7 (bit 7): 1 = Enable reading of logic value on pin RA6 via RAIN6
0 = Disable reading of logic value and guard against floating input levels on pin RA6

RAIEN5 (bit 5): 1 = Enable reading of logic value on pin RA5 via RAIN5
0 = Disable reading of logic value and guard against floating input levels on pin RA5

RAIEN4 (bit 4): 1 = Enable reading of logic value on pin RA4 via RAIN4
0 = Disable reading of logic value and guard against floating input levels on pin RA4

RAIEN3 (bit 3): 1 = Enable reading of logic value on pin RA3 via RAIN3
0 = Disable reading of logic value and guard against floating input levels on pin RA3

RAIEN2 (bit 2): 1 = Enable reading of logic value on pin RA2 via RAIN2
0 = Disable reading of logic value and guard against floating input levels on pin RA2

RAIEN1 (bit 1): 1 = Enable reading of logic value on pin RA1 via RAIN1
0 = Disable reading of logic value and guard against floating input levels on pin RA1

RAIEN0 (bit 0): 1 = Enable reading of logic value on pin RA0 via RAIN0
0 = Disable reading of logic value and guard against floating input levels on pin RA0

RB_IEN (address 7007h): RB input enable register

This register enables the RB pins as inputs.

RB_IEN Register (Address 7007h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RBIEN7	RBIEN6	RBIEN5	RBIEN4	RBIEN3	RBIEN2	RBIEN1	RBIEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RBIEN7 (bit 7): 1 = Enable reading of logic value on pin RB7 via RBIN7 bit
0 = Disable reading of logic value and guard against floating input levels on pin RB7

RBIEN6 (bit 6): 1 = Enable reading of logic value on pin RB6 via RBIN6 bit
0 = Disable reading of logic value and guard against floating input levels on pin RB6

RBIEN5 (bit 5): 1 = Enable reading of logic value on pin RB5 via RBIN5 bit
0 = Disable reading of logic value and guard against floating input levels on pin RB5

RBIEN4 (bit 4): 1 = Enable reading of logic value on pin RB4 via RBIN4 bit
0 = Disable reading of logic value and guard against floating input levels on pin RB4

RBIEN3 (bit 3): 1 = Enable reading of logic value on pin RB3 via RBIN3 bit
0 = Disable reading of logic value and guard against floating input levels on pin RB3

RBIEN2 (bit 2): 1 = Enable reading of logic value on pin RB2 via RBIN2 bit
0 = Disable reading of logic value and guard against floating input levels on pin RB2

RBIEN1 (bit 1): 1 = Enable reading of logic value on pin RB1 via RBIN1 bit
0 = Disable reading of logic value and guard against floating input levels on pin RB1

RBIEN0 (bit 0): 1 = Enable reading of logic value on pin RB0 via RBIN0 bit
0 = Disable reading of logic value and guard against floating input levels on pin RB0

RC_IEN (address 7008h): RC input enable register

This register enables the RC pins as inputs

RC_IEN Register (Address 7008h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RCIEN7	RCIEN6	RCIEN5	RCIEN4	RCIEN3	RCIEN2	RCIEN1	RCIEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RCIEN7 (bit 7): 1 = Enable reading of logic value on pin RC7 via RCIN7 bit
0 = Disable reading of logic value and guard against floating input levels on pin RC7

RCIEN6 (bit 6): 1 = Enable reading of logic value on pin RC6 via RCIN6 bit
0 = Disable reading of logic value and guard against floating input levels on pin RC6

RCIEN5 (bit 5): 1 = Enable reading of logic value on pin RC5 via RCIN5
0 = Disable reading of logic value and guard against floating input levels on pin RC5

RCIEN4 (bit 4): 1 = Enable reading of logic value on pin RC4 via RCIN4 bit
0 = Disable reading of logic value and guard against floating input levels on pin RC4

RCIEN3 (bit 3): 1 = Enable reading of logic value on pin RC3 via RCIN3 bit
0 = Disable reading of logic value and guard against floating input levels on pin RC3

RCIEN2 (bit 2): 1 = Enable reading of logic value on pin RC2 via RCIN2 bit
0 = Disable reading of logic value and guard against floating input levels on pin RC2

RCIEN1 (bit 1): 1 = Enable reading of logic value on pin RC1 via RCIN1 bit
0 = Disable reading of logic value and guard against floating input levels on pin RC1

RCIEN0 (bit 0): 1 = Enable reading of logic value on pin RC0 via RCIN0 bit
0 = Disable reading of logic value and guard against floating input levels on pin RC0

IOCTL (address 7009h): input/output control register

This register enables the predefined pin functions for RA1, RB0, RB1, RA5, RA6, and RA7 pins.

IOCTL Register (Address 7009h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	XEVEN	XINTEN	SMBEN	HDQEN	VOUTEN
Access	—	—	—	R/W	R/W	R/W	R/W	R/W
Reset	—	—	—	0	0	1	0	0

Reserved (bits 7:5): Do not use

XEVEN (bit 4): Enable external event pin
1 = Enable pin RB1 to function as CPU external event pin (RBIEN1 must also be set)
0 = Disable CPU external event functionality for pin RB1

XINTEN (bit 3): Enable external interrupt pin
1 = Enable pin RB0 to function as CPU external interrupt pin (RBIEN0 must also be set)
0 = Disable CPU external interrupt functionality for pin RB0

SMBEN (bit 2): Enable SMBus pins
1 = Enable pins RA7 and RA6 to function as SMB data and SMB clock (RAIEN7 and RAIEN6 must also be set)
0 = Disable SMBus functionality for pins RA7 and RA6

HDQEN (bit 1): Enable HDQ pin
1 = Enable pin RA5 to function as the HDQ communication pin (RAIEN5 must also be set)
0 = Disable HDQ functionality for pin RA5

VOUTEN (bit 0): Enable VOUT pin
1 = Enable pin RA1 to function as the VOUT power source pin
0 = Disable VOUT function for pin RA1

32KOUTEN (address 700ah): 32-kHz output enable register

This register enables the 32-kHz clock to output on pin RC5.

32KOUTEN Register (Address 700ah)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—	—	—	—	—	—	32K_OUT	—
Access	—	—	—	—	—	—	R/W	—
Reset	0	0	0	0	0	0	0	0

Reserved (bits 7:2, 0): Do not use; must be written to zero for proper operation

32K_OUT (bit 1): Enable RC5 to output the 32-kHz clock
1 = Enable RC5 32-kHz clock
0 = Disable 32-kHz output on RC5

NOTE:
When 32K_OUT is enabled, RCOUT5 will be set and cleared according to the state of the 32kHz clock. RCOUT5 will retain the last state of the 32kHz clock output when 32K_OUT is disabled. Writing to RCOUT5 while 32K_OUT is enabled, will not affect the 32kHz clock output on the RC5 pin.

RC_PUP (address 700ch): RC control register

This register enables the internal pullups for the RC pins.

RC_PUP Register (Address 700ch)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RCPUP7	RCPUP6	RCPUP5	RCPUP4	RCPUP3	RCPUP2	RCPUP1	RCPUP0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RCPUP7 (bit 7): 1 = Enable internal pullup for pin RC7
0 = Disable internal pullup for pin RC7

RCPUP6 (bit 6): 1 = Enable internal pullup for pin RC6
0 = Disable internal pullup for pin RC6

RCPUP5 (bit 5): 1 = Enable internal pullup for pin RC5
0 = Disable internal pullup for pin RC5

RCPUP4 (bit 4): 1 = Enable internal pullup for pin RC4
0 = Disable internal pullup for pin RC4

RCPUP3 (bit 3): 1 = Enable internal pullup for pin RC3
0 = Disable internal pullup for pin RC3

RCPUP2 (bit 2): 1 = Enable internal pullup for pin RC2
0 = Disable internal pullup for pin RC2

RCPUP1 (bit 1): 1 = Enable internal pullup for pin RC1
0 = Disable internal pullup for pin RC1

RCPUP0 (bit 0): 1 = Enable internal pullup for pin RC0
0 = Disable internal pullup for pin RC0

control interrupts and events

The bq8015 has two data registers (PFLAG and PIE) for interrupt status and control. These are PFLAG and PIE. The internal CPU STAT register controls the servicing of interrupts.

PFLAG (address 9000h): peripheral flag register

This register signals the status of the various interrupt flags.

PFLAG Register (Address 9000h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMBF	HDQF	ADF	CCF	TIMF	WTF	—	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	—	—
Reset	0	0	0	0	0	0	0	0

SMBF (bit 7): System management bus interrupt flag. This bit signals the SMBus circuit request for interrupt servicing. A controller interrupt to address vector (3h) is generated if SMBIE=GIE=1 when SMBF=1 (sets the CIN bit in the STAT register).

1 = SMBus circuit requests interrupt processing
0 = SMBus request did not occur

HDQF (bit 6): HDQ interrupt flag. This bit signals the HDQ communication circuit request for interrupt servicing. A controller interrupt to address vector (3h) is generated if HDQIE=GIE=1 when HDQF=1 (sets the CIN bit in the STAT register).

1 = HDQ circuit requests interrupt processing
0 = HDQ request did not occur

ADF (bit 5): ADC interrupt flag bit. This bit signals an ADC request for interrupt servicing at the end of a conversion. A controller interrupt to address vector (2h) is generated if ADIE=PINE=GIE=1 when ADF=1 (sets the PIN bit in the STAT register).

1 = ADC circuit requests interrupt processing
0 = ADC request did not occur

CCF (bit 4): CC interrupt flag bit. This bit signals a coulomb counter request for interrupt servicing. A controller interrupt to address vector (2h) is generated if CCIE=PINE=GIE=1 when CCF=1 (sets the PIN bit in the STAT register).

1 = CC circuit requests interrupt processing
0 = CC request did not occur

TIMF (bit 3): Timer interrupt flag. This bit signals a timer request for interrupt servicing. A controller interrupt to address vector (2h) is generated if TIMIE=PINE=GIE=1 when TIMF=1 (sets the PIN bit in the STAT register).

1 = Timer circuit requests interrupt processing once every 7.8125ms (128 times per second)
0 = Timer request did not occur

WTF (bit 2): Wake-timer flag. This bit signals that a wake timeout occurred. The processor exits the halt state if WTE in the PIE register is set.

1 = Wake from internal timer occurred
0 = Timer request did not occur

Reserved (bits 1:0): Do not use.

PIE (address 9001h): peripheral interrupt enable register

This register enables the PIE interrupt from the various registers.

PIE Register (Address 9001h)								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SMBIE	HDQIE	ADIE	CCIE	TIMIE	WTE	XINPOL	XEVPOL
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SMBIE (bit 7): SMBus interrupt enable. This bit enables the SMBus interrupt flag to interrupt the controller. A controller interrupt to address vector (0003h) is generated if SMBF=GIE=1 when SMBIE=1 (sets the CIN bit in the STAT register).

1 = Enable SMBus circuit interrupt requests
0 = Disable SMBus circuit interrupt requests

HDQIE (bit 6): HDQ interrupt enable. This bit enables the HDQ communication flag to interrupt the controller. A controller interrupt to address vector (0003h) is generated if HDQF=GIE=1 when HDQIE=1 (sets the CIN bit in the STAT register).

1 = Enable HDQ circuit interrupt requests
0 = Disable HDQ circuit interrupt requests

ADIE (bit 5): ADC interrupt enable bit. This bit enables an ADC request for interrupt servicing at the end of a conversion. A controller interrupt to address vector (0002h) is generated if ADF=PINE=GIE=1 when ADIE=1 (sets the PIN bit in the STAT register).

1 = Enable ADC interrupt requests
0 = Disable ADC interrupt requests

CCIE (bit 4): CC interrupt enable bit. This bit enables a CC request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if CCF=PINE=GIE=1 when CCIE=1 (sets the PIN bit in the STAT register).

1 = Enable CC interrupt requests
0 = Disable CC interrupt requests

TIMIE (bit 3): Timer interrupt enable. This bit enables a timer request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if TIMF=PINE=GIE=1 when TIMIE=1 (sets the PIN bit in the STAT register).

1 = Enables timer interrupt requests
0 = Disables timer interrupt requests

WTE (bit 2): Wake timer enable interrupt bit. This bit enables WTF in the PFLAG register to set the WEV flag in the cpu STAT register.

1 = Enables the wake timer to restart the controller from HALT
0 = Disables the wake timer from restarting the controller

XINPOL (bit 1): External interrupt polarity select bit. This bit selects the polarity of the external input, active high or active low.

1 = External input is active high
0 = External input is active low

XEVPOL (bit 0): External event polarity select bit. This bit selects the polarity of the external event input, active high or active low.

1 = External event input active high
0 = External event input active low

VTRIM (address a000h): reference voltage trim register

This register stores the trim voltage for the internal bq8015 reference. During a POR or MRST, the trim value for the internal 1.225-V reference is transferred from a reserved flash register to location a000h. This value is used to trim the internal voltage reference.

VTRIM Register (Address a000h)								
	7	6	5	4	3	2	1	0
Name	—	—	—	—	VTRIM3	VTRIM2	VTRIM1	VTRIM0
Access	—	—	—	—	R/W	R/W	R/W	R/W
Reset	—	—	—	—	—	—	—	—

Reserved (bits 7:4): Do not use.

VTRIM3:0 (bits 3:0): Voltage trim values used to digitally adjust the 1.225-V reference. Each bit has a weight of approximately 3.7 mV.

internal CPU register description

The bq8015 has 16 internal CPU registers. Refer to the *bq80xx Core Details Manual User's Guide* (TI literature number SLUU090) for a complete description. The status register is used in conjunction with several of the bq8015 peripherals and is included for ease of reference.

STAT (address eh): internal CPU status register

This internal CPU register is used to enable interrupts and monitor their status.

STAT Register (Internal CPU Register: eh)								
	7	6	5	4	3	2	1	0
Name	PINE	XINE	GIE	PIN	XIN	CIN	XEV	WEV
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	—	—	0	—	—	—	—	—

PINE (bit 7): Peripheral interrupt enable bit. This bit enables a controller interrupt when PIN and GIE are asserted.

1 = PIN enabled to generate an interrupt if GIE=1

0 = PIN inhibited from generating an interrupt

XINE (bit 6): External interrupt enable bit. This bit enables a controller interrupt when XIN and GIE are asserted.

1 = XIN enabled to generate an interrupt if GIE=1

0 = XIN inhibited from generating an interrupt

GIE (bit 5): Global interrupt enable bit. This bit disables all interrupts when cleared. GIE is automatically cleared when an interrupt service routine is executed to prevent unwanted interrupt nesting.

1 = Allows PIN, XIN, and CIN interrupts to be processed by the controller

0 = Disables all interrupts

PIN (bit 4): Peripheral interrupt bit (lowest priority). This bit signals a peripheral circuit request for interrupt service.

1 = Peripheral circuit interrupt requested

0 = No peripheral interrupt service requested

STAT (address eh): internal CPU status register (continued)

XIN (bit 3): External interrupt bit (medium priority). This bit signals an external interrupt service request that was received via the INT (RB0) pin.

1 = External interrupt service requested

0 = No external interrupt service requested

CIN (bit 2): Communication interrupt bit (highest priority).This bit signals a communication circuit request for interrupt service.

1 = Communication circuit interrupt requested from the HDQ or SMBus

0 = No communication interrupt service requested

XEV (bit 1): External event bit. This bit signals that an external wake-timer event occurred via the EV (RB1) pin that can wake the controller from a HALT state.

1 = External event occurred

0 = External event has not occurred

WEV (bit 0): Wake event bit. This bit signals a wake timer event occurred that can wake the controller from a HALT state.

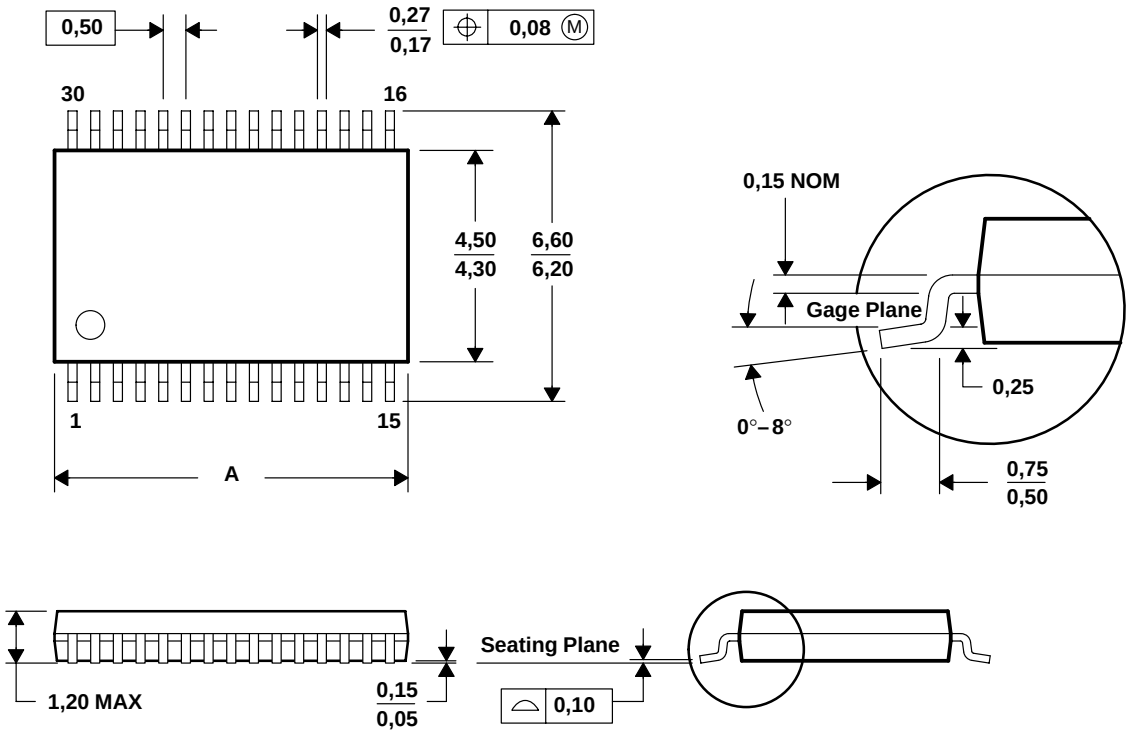
1 = Internal event occurred

0 = Internal wake timer event has not occurred

MECHANICAL DATA

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,10	12,60
A MIN	7,70	7,70	9,60	10,90	12,40

4073252/D 09/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ8015DBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ8015DBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ8015DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ8015DBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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